UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2015/2016

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME	:	BACHELOR OF ELECTRICAL ENGINEERING WITH HONOURS/ BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	:	DECEMBER 2015 / JANUARY 2016
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX I** WITH YOUR ANSWER BOOKLET 3. STUDENT ARE **NOT ALLOWED** TO BRING OUT THE QUESTION PAPER

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) The compact disk (CD) player is an example of a system in which both digital and analog circuits are used. Explain the basic principle using appropriate block diagram.

(4 marks)

(b) Solve the following:

(i) Convert the binary number 0.0110 to decimal.

(2 marks)

(ii) Convert the hexadecimal $6AC6.23_{16}$ to octal.

(2 marks)

(c) Given the Boolean expression

$$Z = \overline{\overline{PQ}(RS + P\overline{S})(\overline{PQ} + \overline{RS})}$$

(i) Draw the logic circuit from the Boolean equation.

(5 marks)

(ii) Simplify expression Z using Boolean theorem.

(5 marks)

(iii) Implement the function Z in **Q2(c)(ii)** using only a 2-input NAND gates.

(5 marks)

Q2 Design an electronic circuit that implement the function of Z = 3X+Y. The circuit takes two 2-bit binary numbers X(x1, x0) and Y(y1, y0) for their inputs and produces an output binary number Z(z3, z2, z1, z0).

(20 marks)

Q3 **Figure Q3** shows how an eight-input multiplexer can be used to generate a four-variable logic function, even though the multiplexer has only three SELECT inputs.

(a) Analyse and build the truth table for this circuit.

(12 marks)

(b) Write the Boolean expression of this circuit. You do not need to simplify the expression.

(3 marks)

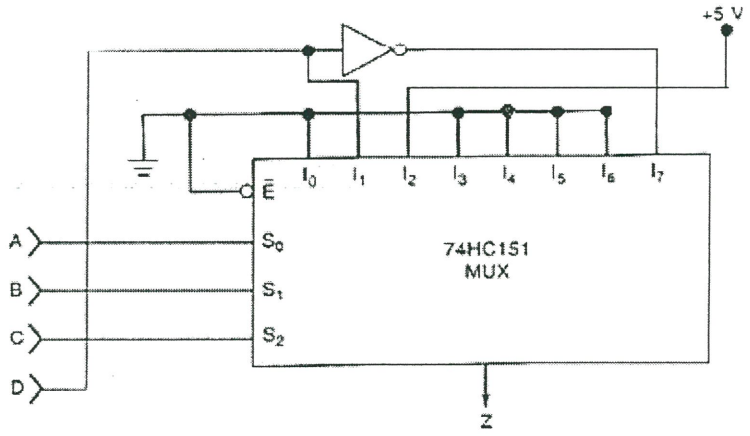

FIGURE Q3

Q4 (a) Explain the differences in S-R and J-K flip flop's operation.

(4 marks)

(b) Given the circuit diagram of **Figure Q4(a)**, complete the timing diagram for Q_A, Q_B and Q_C of **Figure Q4(b)** in **APPENDIX 1**. Assume that Q_A, Q_B and Q_C are at high level initially.

(10 marks)

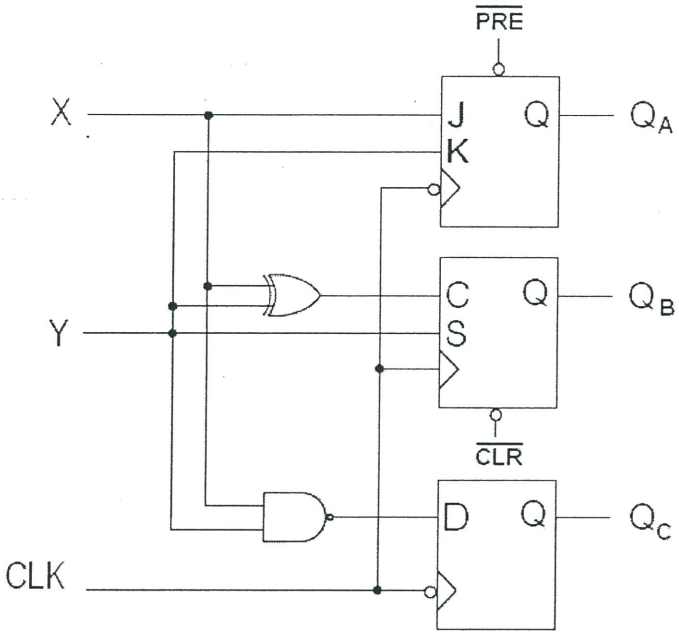

FIGURE Q4(a)

Q5 (a) Design a MOD-12 asynchronous counter using JK flip-flop shown in **Figure Q5(a)**. Show your steps clearly.

(10 marks)

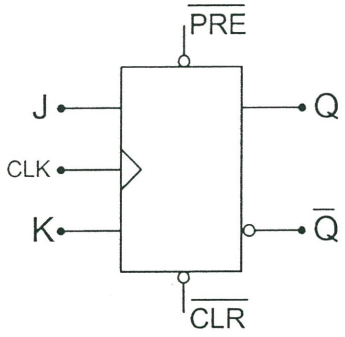

FIGURE Q5(a)

(b) **Figure Q5(b)** shows the state transition diagram of a state machine.

(i) Build the excitation table for this state machine. Use JK flip-flops.

(8 marks)

(ii) Find the simplest Boolean expression for the circuit using Karnaugh map.

(6 marks)

(iii) Draw the circuit.

(4 marks)

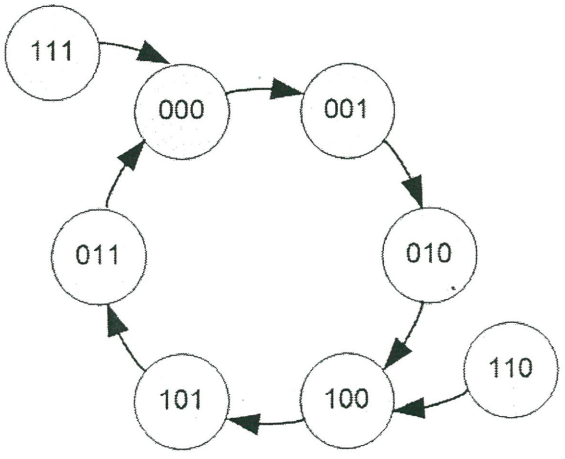

FIGURE Q5(b)

- END OF QUESTION –

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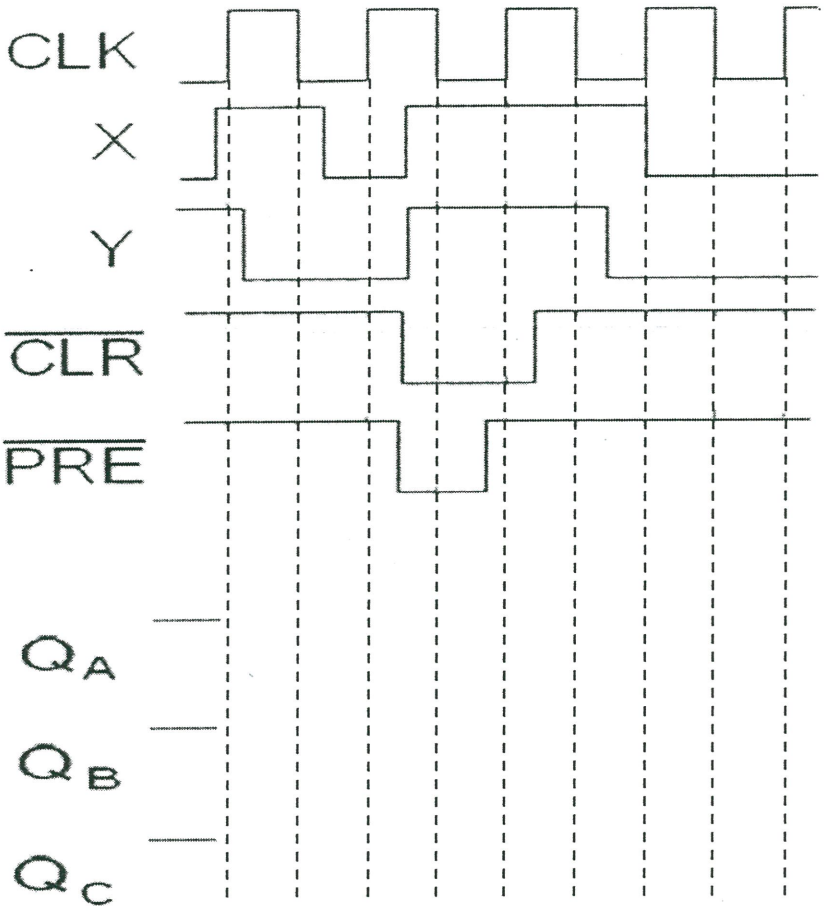

FIGURE Q4(b)