Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2014/2015

COURSE NAME	:	DIGITAL TECHNIQUES
COURSE CODE	:	BEF 12302
PROGRAMME	:	BACHELOR OF ELECTRICAL ENGINEERING WITH HONOURS
EXAMINATION DATE	:	JUNE 2015 / JULY 2015
DURATION	:	2 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS.
		2. ATTACH APPENDIX A, B AND C WITH YOUR ANSWER BOOKLET.

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) Due to the large size of data, some digital systems employ an error detection method known as parity bit. State the **TWO (2)** types of parity bit method and explain both methods using a clear example to send an 8-bit code.

(6 marks)

(b) Convert the hexadecimal number 1D6 to BCD code.

(6 marks)

(c) Convert the octal number 2675 to Gray code.

(6 marks)

(d) From the following maxterm expansion, obtain a minimum Sum-of-products (SOP) expression.

$$F(W,X,Y,Z) = \prod M(0,2,3,4,8,9,10)$$

(7 marks)

Q2 (a) By using Boolean theorem, prove that

$$(A+B+\overline{C})\cdot(A+\overline{B}+C)\cdot(\overline{A}+B+C)\cdot(\overline{A}+\overline{B}+\overline{C}) = \overline{A \oplus B \oplus C}$$

(6 marks)

(b) Given the Boolean expression

$$Z = \overline{A \cdot B} + A \cdot B \cdot C \cdot D + (A \oplus D)$$

(i) Draw the Karnaugh map

(5 marks)

(ii) Determine the minimum Sum of Product expression for Z.

(5 marks)

(iii) Draw the combinational logic circuit for Z.

(4 marks)

(c) A NAND gate is a universal gate. Using Boolean algebra, prove that the circuit shown in Figure **Q2(c)** can be reduced to a single gate.

(5 marks)

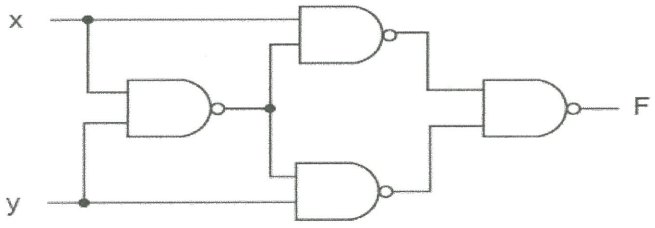

FIGURE Q2(c)

Q3 (a) Describe the operation of the following functional combinational logic circuit. You may use appropriate diagram and truth table to aid your explanation.

i) Multiplexers.

(2 marks)

ii) Comparators

(2 marks)

(b) Implement the following Boolean expression using IC 74LS151 (8 line-to-1 line multiplexer) in **APPENDIX A**. Symbol for IC 74LS151 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS151 (8 line-to-1 line multiplexer).

$$Z = \overline{(A + B)} + C$$

(5 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **APPENDIX B**. Symbol for IC 74LS138 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder).

$$f_1(x_2, x_1, x_0) = \sum m(0,1,5,6,7)$$

$$f_2(x_2, x_1, x_0) = \prod M(2,3,4,5,7)$$

(8 marks)

(d) Complete the missing entries (i), (ii), (iii), (iv), (v), (vi), (vii) and (viii) in Table **Q3(d)** of flip-flop excitation values required to produce the indicated flip-flop state changes, where X indicates the present state and Y is the desired next state of the flip-flop.

(8 marks)

TABLE Q3(d)

Present state	**Next State**	**J-K Flip flop**		**SC Flip flop**		**D Flip flop**
X	**Y**	**J**	**K**	**S**	**C**	**D**
0	0	(i)	(ii)			(iii)
1	0			(iv)	(v)	
0	1	(vi)	(vii)			
1	(viii)	1	0			

Q4 (a) State machine is important to demonstrate operation of a sequential circuit. There are two main types which known as Moore Model and Mealy Model. Briefly compare two types of state machine stated above.

(4 marks)

(b) Figure **Q4(b)(i)** shows a logic circuit that comprises of a JK flip-flop, an OR gate and an inverter. Figure **Q4(b)(ii)** shows the waveforms for signal CLK, J, K, $\overline{PRE}$ and $\overline{CLR}$. Complete the timing diagram for Q in **APPENDIX C** and write down the operation (e.g. HOLD) that takes place in each clock pulse as illustrated in the diagram.

(7 marks)

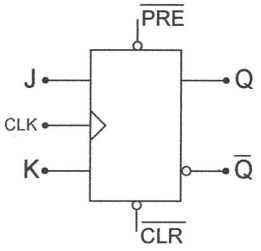

FIGURE Q4(b)(i)

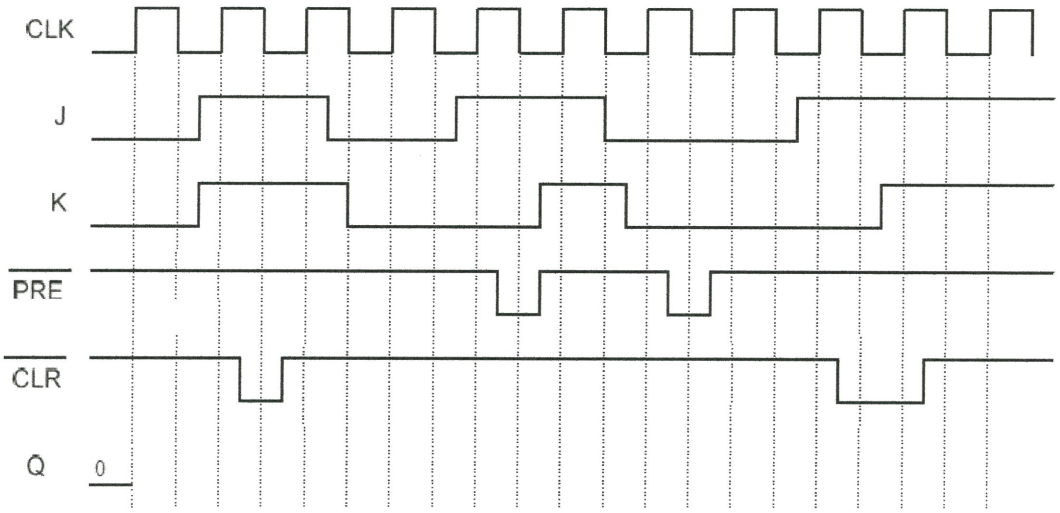

FIGURE Q4(b)(ii)

(c) Determine the count sequence for the counter shown in Figure **Q4(c)** by providing the next state table. Also draw a state diagram for it. Deduce the state(s) whereby the counter will always remain there.

(10 marks)

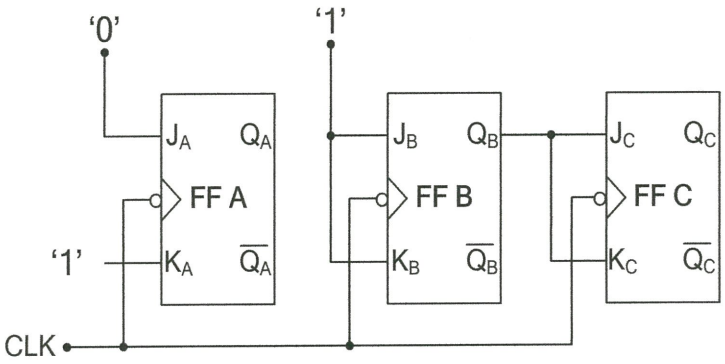

FIGURE Q4(c)

(d) Explain the operation of the Serial In Parallel Out (SIPO) register and Serial In Serial Out (SISO) register.

(4 marks)

-END OF QUESTION-

FINAL EXAMINATION

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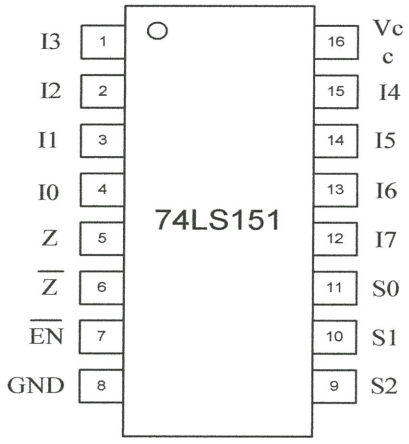
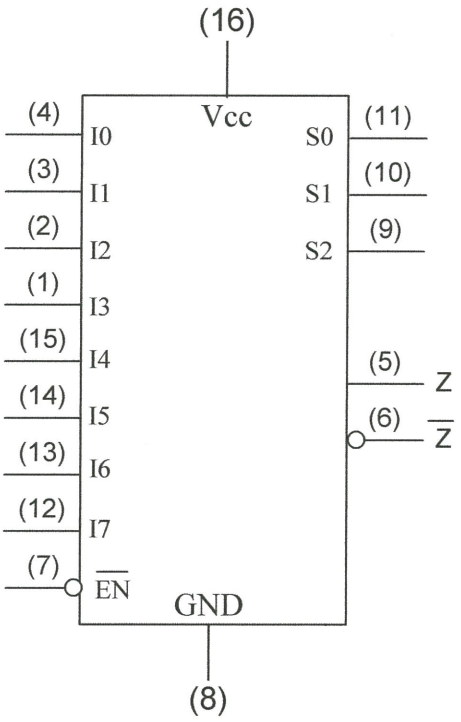
COURSE : DIGITAL TECHNIQUES COURSE CODE : BEF12302

APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS151 (8-to-1 Multiplexer)





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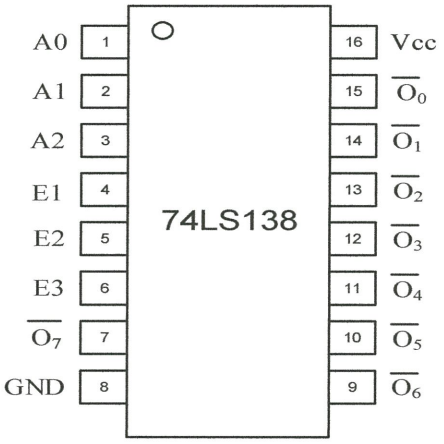
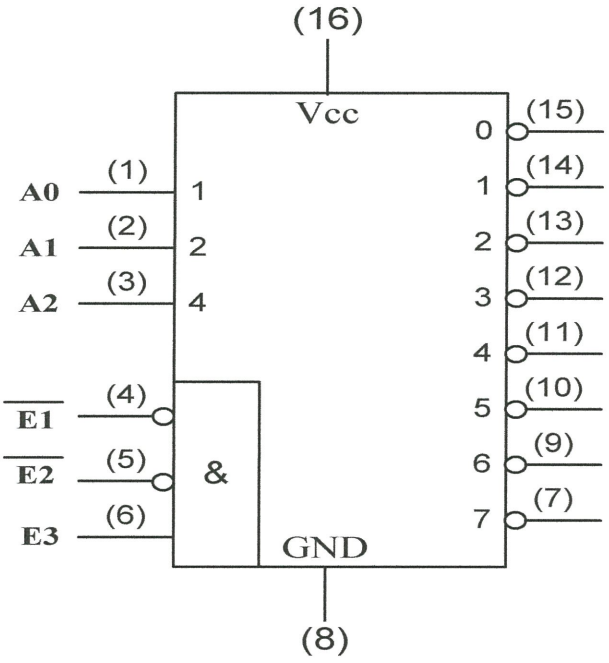
APPENDIX B

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS138 (3-to-8 Decoder)





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APPENDIX C