Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2014/2015

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME	:	BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	:	JUNE 2015 / JULY 2015
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) List the key technology in each of the four generations of computer evolution.
(4 marks)

(b) Write the sequence of instructions for stack operation to perform the following computation:

(2)/(4)+(8)*(3)

(7 marks)

(c) Determine the suitable addressing mode for each of the given register transfer notations below:

(i) R5 <- R5 + R3
(2 marks)

(ii) R1 <- R4 + 3
(2 marks)

(iii) R8 <- R7 + M[R6]
(2 marks)

Q2 Several instructions will be executed by Intel Xeon processor having 4-stage pipelined architecture. The instruction cycle comprises 4 steps; fetch (F), decode (D), execute (E), and write back (W) where all steps require 1 clock cycle except execute (E) step which takes 2 clock cycles. Assume 1 clock cycle = 5 ns.

(a) Sketch the space time diagram to execute four (4) instructions.
(6 marks)

(b) Calculate the total execution time (in nanosecond) needed by the pipelined computer to execute a C++ program having 1500 instructions.
(4 marks)

(c) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in Q2(ii).
(4 marks)

(d) A C++ program having a total of 1500 instructions has 25 sequence of LOAD-LOAD-ADD-MULT instructions (total instructions in the sequence is 100) from the total 1500 instructions (that means LOAD-LOAD-ADD-MULT-LOAD-LOAD-ADD-MULT until 25 times). The MULT instruction needs an operand from the results of ADD instruction stored in same register (R4) creating a data hazard. To solve this, a two-cycle stall must be added before executing MULT instruction in each of the 25 instruction sequences. Determine the new performance speed up of the pipelined computer over non-pipelined computer.
(4 marks)

Q3 (a) Sketch the typical memory hierarchy in a computer system.

(5 marks)

(b) Describe the reasons of using memory hierarchy in computer architecture.

(4 marks)

(c) Describe one advantage and disadvantage when using SRAM for cache memory.

(2 marks)

Q4 (a) Explain the following concepts to determine cache performance:

(i) Hit rate

(1 mark)

(ii) Miss rate

(1 mark)

(iii) Miss penalty

(1 mark)

(b) From the diagram shown in Table **Q4**, determine the miss penalty when an L1 cache miss occurs.

TABLE Q4

Memory Level	Access Time (ns)
L1 cache	10
L2 cache	15
L3 cache	20
DDR SDRAM	50
Hard disk	200

(2 marks)

(c) The miss rate when executing a software application is 77% with 50 ns miss penalty. Propose two (2) methods to improve the miss rate and miss penalty.

(6 marks)

Q5 (a) A large amount data needs to be transferred from a host computer to an I/O storage device using very high data transfer bandwidth (more than 1 Gb/s). Suggest a bus communication protocol to be used for the specified data transfer operation. Support your answer with two (2) reasons.

(6 marks)

(b) Differentiate between memory-mapped IO, isolated IO, and interrupt-driven IO.

(6 marks)

(c) Explain the advantages and disadvantages of asynchronous bus.

(4 marks)

Q6 For the 64K x 8, 16M x 32, and 4G x 64 memory units, determine:

(a) The number of address lines

(3 marks)

(b) Data lines

(3 marks)

(c) The number of bytes that can be stored in the specified memory

(3 marks)

Q7 (a) Distinguish between compiler, assembler, and debugger in a computer system.

(6 marks)

(b) An engineer has written a C program and compiled it with two different compilers. Each compiler generated the following numbers of instructions which comprise three instruction types; A, B, and C for this program (M = million):

Compiler 1: A = 5M, B = 1M, C = 1M
Compiler 2: A = 10M, B= 1M, C = 1M

Assume the clock speed of the processor executing the program is 1 GHz. An instruction of type A, B, and C takes 1, 2, and 3 clock cycles respectively. Answer the following questions:

(i) Calculate the execution time for compiler 1 and compiler 2.

(4 marks)

(ii) Calculate the million instructions per second (MIPS) for compiler 1 and compiler 2.

(4 marks)

(iii) Summarize the results of the calculation.

(4 marks)

– END OF QUESTIONS –