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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2014/2015

COURSE NAME	:	ADVANCED MICROCONTROLLER
COURSE CODE	:	BEC 41103
PROGRAMME	:	BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	:	JUNE 2015 /JULY 2015
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER ALL QUESTIONS

THIS PAPER CONSISTS OF **FOURTEEN (14)** PAGES

Q1 (a) Microcontroller is widely used to build embedded system products.

(i) State components that usually put together with the microcontroller onto a single chip.

(2 marks)

(ii) Explain Harvard architecture and how it makes processing of code and data faster

(3 marks)

(iii) Discuss the drawback of using Harvard architecture for memories external to the CPU?

(2 marks)

(b) A door sensor is connected to the RB1 pin, and a buzzer is connected to RC7. When open the door, the buzzer will sound by a square wave of 200 Hz frequency. Assume the crystal frequency is 4MHz.

(i) Determine the instruction time cycle time.

(3 marks)

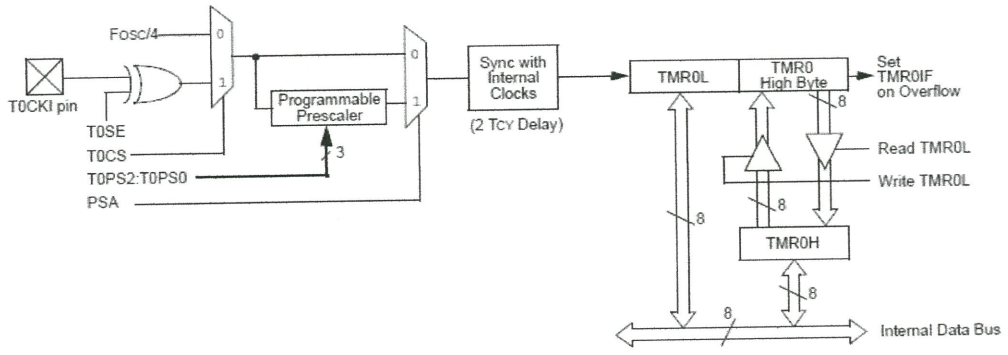
(ii) Determine the function for the delays.h library that used to generate the square wave.

(3 marks)

(iii) Construct a C program to monitor the door sensor and sound the buzzer by the square wave of 200Mhz frequency when the door opens. Consider the program is implemented at PIC18F4520.

(7 marks)

Q2 (a) Figure **Q2 (a)** shows block diagram for 16-bit Timer0.



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Figure Q2(a) : Timer0 16-bit block diagram

(i) State the contents of the TMR0H:TMR0L and TMR0IL bit upon reset the PIC18F4520.

(2 marks)

(ii) Explain the usage of TMR0IF bit in Timer0.

(2 marks)

(iii) Assuming that XTAL = 10MHz is utilized to generate a square wave on pin RB2, justify the lowest and the highest square wave frequency that can be generated using Timer0 in 16-bit mode.

(4 marks)

(b) Analyze and discuss the C code as given below. Highlight 12 points concerning the purpose and functionality for the code in Figure Q2 (b).

```
#include<P18f4520.h>
void main (void)
{
   TRISAbits.TRISA4 = 1;
   TRISB = 0;
   TRISD = 0;
   T0CON = 0X25;
   TMR0H =0;
   TMR0L =0;

   while (1)
     {
       do
        {
          T0CONbits.TMR0ON = 1;
          PORTB = TMR0L;
          PORTD = TMR0H;
        }
       while (INTCONbits.TMR0IF = = 0);
       T0CONbits.TMR0ON = 0;
       INTCONbits.TMR0IF = 0;
     }
}
```

Figure Q2 (b)

(12 marks)

Q3 (a) The PIC18 transfers and receives data serially at many different baud rates. The baud rate is programmable with the 8-bit register called SPBRG.

(i) For XTAL = 10 MHz, calculate the SPBRG value (in both decimal and hex) for baud rates 9600.

(3 marks)

(ii) Investigate the SPBRG value (in both decimal and hex) for Q3(a)i. Given that BRGH bit of TXSTA register is HIGH.

(3 marks)

(iii) Calculate the baud rate error for Q3(a)i.

(2 marks)

(b) Create a C program based on the following statement:
"PIC18 gets data from PORTD and sends it to TXREG continuously while incoming data from the serial port is sent to PORTB. Assume that XTAL = 10MHz and the baud rate = 9600."

(12 marks)

Q4 (a) Explain the conversion time in ADC operation.

(5 marks)

(b) Analyse the program as given in Figure Q4(b). Then, answer all the questions from Q4(b)(i) to Q4(b)(v).

```
#include <p18f458.h>
void EE_WRT(void);
unsigned char EE_READ (void);
void SerTx (unsigned char);

void main ( )
 {
   rom far char* RomPointer ="MOVE ME";
   char RamString [7];
   unsigned char x, ch, k = sizeof (RomPointer);
   TXSTA = 0x20;
   SPBRG = 15;
   TXSTAbits.TXEN =1;
   RCSTAbits.SPEN =1;

   for(x=0;x<7;x++)
    {
      RamString[x] = RomPointer [x];
    }

   for(x=0;x<7;x++)
    {
      EEADR =x;
      EEDATA = RamString [x];
      EE_WRT ( ) ;
    }

   EECON1bits.WREN = 0;
   for (x =0; x<7;x++)
    {
      EEADR = x;
      ch = EE_READ ( );
      SerTx (ch);
     }
   while (1);
 }

void EE_WRT( )
```

```
{
  EECON1bits.EEPGD = 0;
  EECON1bits.CFGS = 0;
  EECON1bits.WREN = 1;
  INTCONbits.GIE = 0 ;
  EECON2 = 0x 55;
  EECON2 = 0xAA;
  EECON1bits.WR = 1;
  INTCONbits.GIE = 1;
  while (!PIR2bits.EEIF);
  PIR2bits.EEIF = 0;
}

unsigned char EE_READ( )
 {
  EECON1bits.EEPGD =0;
  EECON1bits.CFGS = 0;
  EECON1bits.RD =1;
  return (EEDATA);
 }

void SerTx(unsigned char c)
 {
  while(PIR1bits.TX1F = = 0);
  TXREG = c;
 }
```

Figure Q4(b)

(i) Examine the setting of all registers in subroutine main.

(2 marks)

(ii) Explain the functionality of for-loop in main subroutine.

(3 marks)

(iii) Explain the process for writing data into the EEPROM according to EE_WRT( ) subroutine.

(2 marks)

(iv) Describe the reading process in the program.

(2 marks)

(v) Evaluate the objective of SerTx subroutine.

(1 mark)

(c) Decide the last step for writing to EEPROM. Evaluate the purpose of the step that you mention?

(5 marks)

Q5 (a) There are three (3) factors that affect the speed of the motor. List all of them.

(3 marks)

(b) Propose a solution to operate the motor using PWM if the microcontroller does not have PWM circuitry.

(2 marks)

(c) State an advantage of DC motors than AC motors.

(3 marks)

(d) Construct a C code for Full-Bridge implementation of the PWM for ECCP module.

(10 marks)

(e) Evaluate the importance of driver that will be connected between microcontroller and relay.

(2 marks)

-END OF QUESTIONS-

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PROGRAMME : BEJ
COURSE CODE : BEC41103

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

T0CON (TIMER0 control register)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

INTCON register

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PROGRAMME : BEJ
COURSE CODE : BEC41103

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **PSPIF:** Parallel Slave Port Read/Write Interrupt Flag bit(1)
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

Note 1: This bit is unimplemented on 28-pin devices and will read as '0'.

bit 6 **ADIF:** A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit
1 = The EUSART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The EUSART receive buffer is empty

bit 4 **TXIF:** EUSART Transmit Interrupt Flag bit
1 = The EUSART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The EUSART transmit buffer is full

bit 3 **SSPIF:** Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode.

bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

PIR1 (Peripheral interrupt request (flag) register 1)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in Sync mode.

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data
Can be address/data bit or a parity bit.

TXSTA (Transmit Status and Control Register)

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PROGRAMME : BEJ
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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **RX9:** 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.

bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-bit (RX9 = 0):
Don't care.

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D:** 9th bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

RCSTA (Receive Status and Control register)

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PROGRAMME : BEJ
COURSE CODE : BEC41103

BAUD RATE (Kbps)	Fosc = 40 MHz		SPBRG value (decimal)	33 MHz		SPBRG value (decimal)	25 MHz		SPBRG value (decimal)	20 MHz		SPBRG value (decimal)
	KBAUD	% ERROR		KBAUD	% ERROR		KBAUD	% ERROR		KBAUD	% ERROR	
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	2.40	-0.07	214	2.40	-0.15	162	2.40	+0.16	129
9.6	9.62	+0.16	64	9.55	-0.54	53	9.53	-0.76	40	9.47	-1.36	32
19.2	18.94	-1.36	32	19.10	-0.54	26	19.53	+1.73	19	19.53	+1.73	15
76.8	78.13	+1.73	7	73.66	-4.09	6	78.13	+1.73	4	78.13	+1.73	3
96	89.29	-6.99	6	103.13	+7.42	4	97.66	+1.73	3	104.17	+8.51	2
300	312.50	+4.17	1	257.81	-14.06	1	NA	-	-	312.50	+4.17	0
500	625	+25.00	0	NA	-	-	NA	-	-	NA	-	-
HIGH	625	-	0	515.63	-	0	390.63	-	0	312.50	-	0
LOW	2.44	-	255	2.01	-	255	1.53	-	255	1.22	-	255

BAUD RATE (Kbps)	Fosc = 16 MHz		SPBRG value (decimal)	10 MHz		SPBRG value (decimal)	7.15909 MHz		SPBRG value (decimal)	5.0688 MHz		SPBRG value (decimal)
	KBAUD	% ERROR		KBAUD	% ERROR		KBAUD	% ERROR		KBAUD	% ERROR	
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.20	+0.16	207	1.20	+0.16	129	1.20	+0.23	92	1.20	0	65
2.4	2.40	+0.16	103	2.40	+0.16	64	2.38	-0.83	46	2.40	0	32
9.6	9.62	+0.16	25	9.77	+1.73	15	9.32	-2.90	11	9.90	+3.13	7
19.2	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5	19.80	+3.13	3
76.8	83.33	+8.51	2	78.13	+1.73	1	111.86	+45.65	0	79.20	+3.13	0
96	83.33	-13.19	2	78.13	-18.62	1	NA	-	-	NA	-	-
300	250	-16.67	0	156.25	-47.92	0	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	250	-	0	156.25	-	0	111.86	-	0	79.20	-	0
LOW	0.98	-	255	0.61	-	255	0.44	-	255	0.31	-	255

BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit(1)
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6 **ADIE**: A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5 **RCIE**: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE**: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSPIE**: Master Synchronous Serial Port Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0 **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

PIE1 (PERIPHERAL INTERRUPT ENABLE REGISTER 1)

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PROGRAMME : BEJ
COURSE CODE : BEC41103

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	$\overline{WR}$	$\overline{RD}$
bit 7							bit 0

bit 7 **EEPGD:** Flash Program or Data EEPROM Memory Select bit
1 = Access program Flash memory
0 = Access data EEPROM memory

bit 6 **CFGS:** Flash Program/Data EE or Configuration Select bit
1 = Access Configuration registers
0 = Access program Flash or data EEPROM memory

bit 5 **Unimplemented:** Read as '0'

bit 4 **FREE:** Flash Row Erase Enable bit
1 = Erase the program memory row addressed by TBLPTR on the next $\overline{WR}$ command (reset by hardware)
0 = Perform write only

bit 3 **WRERR:** Write Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{MCLR}$ or any WDT Reset during self-timed programming in normal operation)
0 = The write operation completed

Note: When a WRERR occurs, the EEPGD or FREE bits are not cleared. This allows tracing of the error condition.

bit 2 **WREN:** Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the EEPROM or Flash memory

bit 1 $\overline{WR}$: Write Control bit
1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle (The operation is self-timed and the bit is cleared by hardware once write is complete. The $\overline{WR}$ bit can only be set (not cleared) in software.)
0 = Write cycle is complete

bit 0 $\overline{RD}$: Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. $\overline{RD}$ is cleared in hardware. The $\overline{RD}$ bit can only be set (not cleared) in software. $\overline{RD}$ bit cannot be set when EEPGD = 1.)
0 = Does not initiate an EEPROM read

EECON1 (EEPROM CONTROL REGISTER 1)