Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME	: DIGITAL TECHNIQUES
COURSE CODE	: BEF12302
PROGRAMME	: BEV
EXAMINATION DATE	: JUNE 2014
DURATION	: 2 HOURS
INSTRUCTION	: A) ANSWER **ALL** QUESTIONS
	: B) ATTACH APPENDICES A AND B WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) Digital systems must be able to handle both positive and negative numbers. A signed binary number consists of both sign and magnitude information. The sign indicates the number is positive or negative and while the magnitude is the value of the number. Express the decimal number -1510 as an 8-bit binary number,

(i) in the sign-magnitude form. Show all the steps.

(1 mark)

(ii) in the 1's complement form. Show all the steps.

(1 mark)

(iii) in the 2's complement form. Show all the steps.

(2 marks)

(b) Convert the decimal number 53.875 to binary and hexadecimal number.

(3 marks)

Q2 (a) Figure **Q2** shows an even parity generator circuit for a 4-bit input, A, B, C and D.

(i) Determine the output (Z) if the inputs are A=0, B=1, C=1 and D=0.

(1 mark)

(ii) Develope the truth table for this even parity generator circuit.

(4 marks)

(iii) Determine the minimum Sum of Product expression for Z.

(4 marks)

(iv) Draw the combinational logic circuit for Z, using exclusive-OR gates.

(2 marks)

(b) Using only 2 inputs NAND gate, draw the circuit to implement the following function:

$$Z = A \oplus B$$

(4 marks)

Q3 (a) Describe the operation of the following functional combinational logic circuit. You may us e appropriate diagram and truth table to aid your explanation.

(i) Multiplexer

(2 marks)

(ii) Decoder

(2 marks)

(b) Implement the following Boolean expression using IC 74LS151 (8 line-to-1 line multiplexer) in **APPENDIX A**. Symbol for IC 74LS151 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS151 (8 line-to-1 line multiplexer).

$$Z = A \oplus B \oplus C$$

(4 marks)

Q4 (a) Figure **Q4(b)** show the waveforms for signal CLK, J, K, asynchronous input $\overline{PRE}$ and $\overline{CLR}$. These signals are applied to the positive edge-triggered J-K flip-flop circuit shown in Figure **Q4(a)**. Complete the timing diagram for Q in **APPENDIX B**. Assume that Q is initially LOW.

(3 marks)

(b) A clock generator system has an input frequency of 36 kHz. The system is required to generate two frequencies, 9 kHz and 3 kHz at the outputs. To generate the two output frequencies, two frequency divider circuits are required. Identify the modulos of counter for the two frequency divider circuits.

(2 marks)

(c) Figure **Q4(c)** shows the state transition diagram of a state machine.

(i) Build the excitation table for this state machine. Use JK Flip-flop.

(6 marks)

(ii) Using Karnaugh map method, obtain the simplest Boolean expression for the circuit.

(6 marks)

(iii) Draw the circuit implementation for answer in part Q4(c)(ii).

(3 marks)

- END OF QUESTIONS

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2013/2014 PROGRAMME: BEV
COURSE NAME: DIGITAL TECHNIQUES COURSE CODE: BEF12302

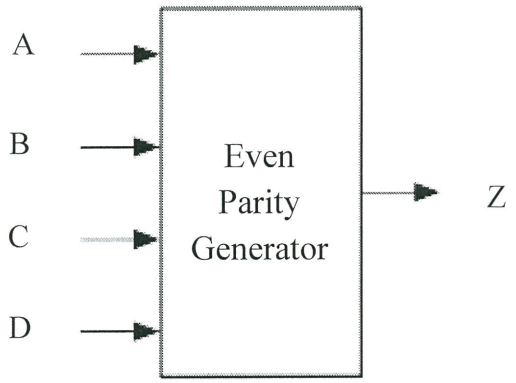


FIGURE Q2

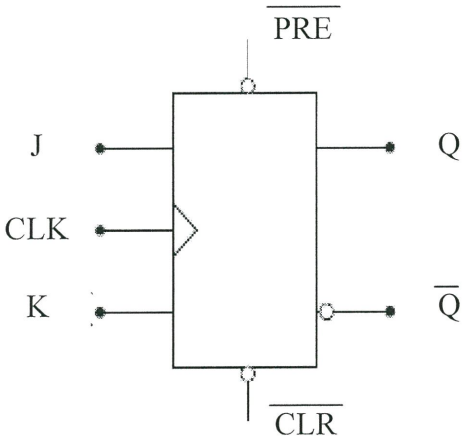


FIGURE Q4(a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2013/2014 PROGRAMME: BEV
COURSE NAME: DIGITAL TECHNIQUES COURSE CODE: BEF12302

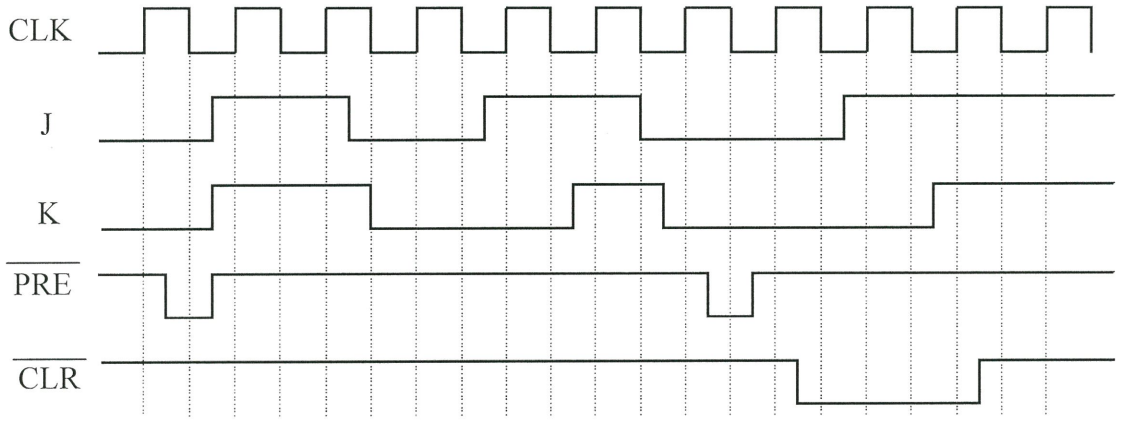


FIGURE Q4(b)

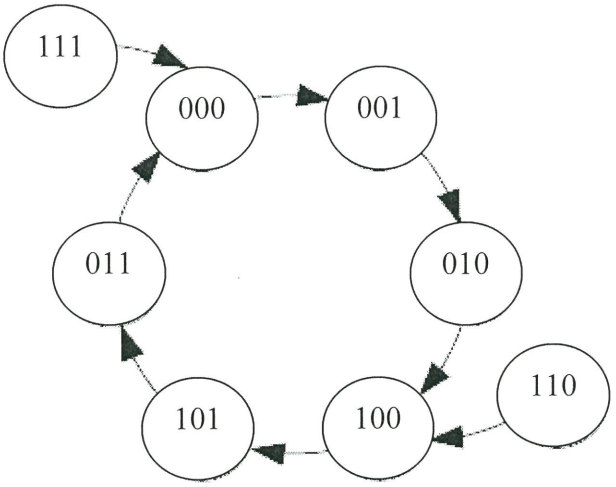


FIGURE Q4(c)

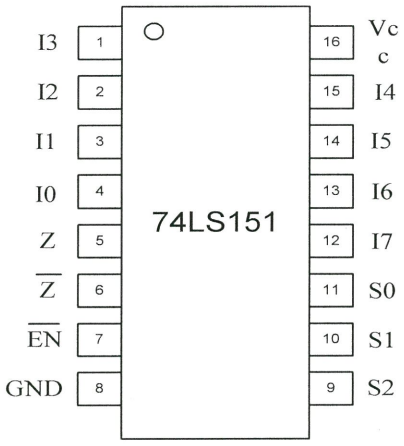
FINAL EXAMINATION

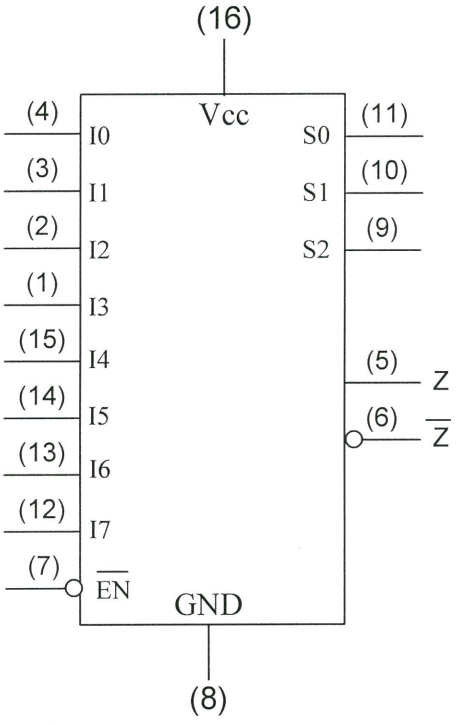
SEMESTER/SESSION: SEM II/2013/2014 PROGRAMME: BEV
COURSE NAME: DIGITAL TECHNIQUES COURSE CODE: BEF12302

APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS151 (8-to-1 Multiplexer)





FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2013/2014 PROGRAMME: BEV
COURSE NAME: DIGITAL TECHNIQUES COURSE CODE: BEF12302

APPENDIX B