Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME	:	2BEJ
EXAMINATION DATE	:	JUNE 2014
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX I, II AND III** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **ELEVEN (11)** PAGES

Q1 (a) List two advantages of digital data as compared to analog data.

(4 marks)

(b) Prove the following Boolean expression.

(i) $(A+B+\overline{C})(\overline{A}+\overline{B}+\overline{C}) = A \oplus B+\overline{C}$

(4 marks)

(ii) $(A+C)(A+\overline{B}) = AB+\overline{A}C$

(4 marks)

(c) The logic circuit showed in Figure **Q1 (c)** generates an output, MEM that is used to activate the memory ICs in particular microcomputer. Determine the input conditions necessary to activate MEM.

(3 marks)

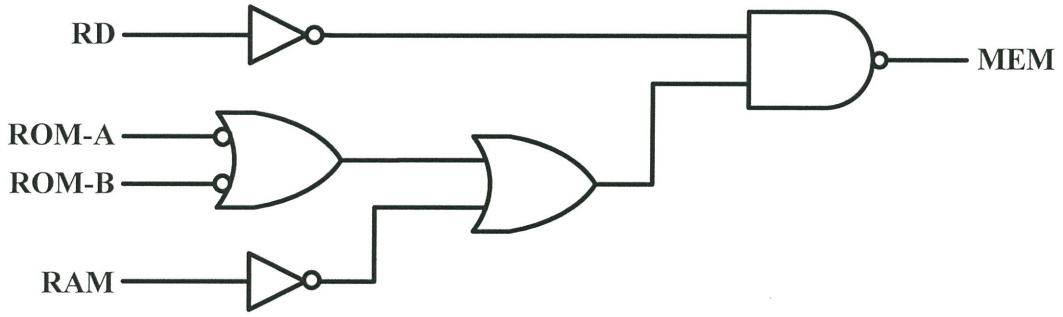

FIGURE Q1 (c)

Q2 (a) Differentiate the characteristic of four main categories of 4-bit registers in terms of data propagation.

(5 marks)

(b) $(\bar{A} + \bar{C})(C + D)$ is simplified Boolean expression of the following expression;

$$Z = \bar{A}\bar{B}D + BC\bar{D} + \bar{A}C\bar{D}$$

Determine if there are any 'don't care' entries.

(5 marks)

(c) Figure **Q2 (c)** shows a 4-bit counter with a specific MOD. MR input is used to reset all flip-flop to LOW.

(i) State the MOD of counter

(1 marks)

(ii) Sketch the timing diagram for Q_0, Q_1, Q_2 and Q_3 in the **APPENDIX I**.

(4 marks)

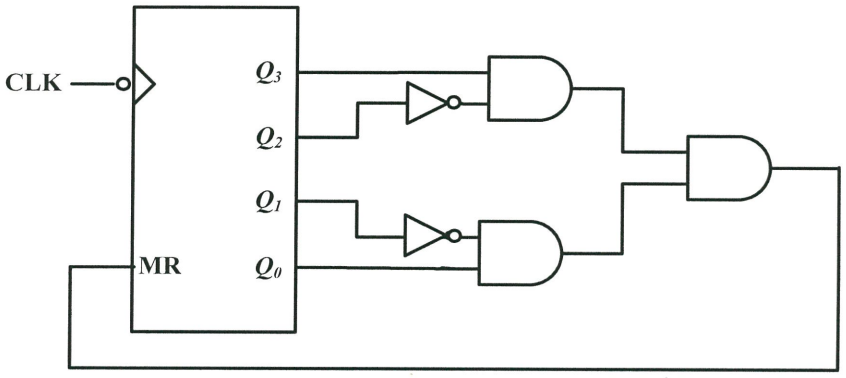

FIGURE Q2 (c)

Q3 (a) State the differences between Mealy machine and Moore machine

(4 marks)

(b) Figure **Q3 (b)** shows a state machine implemented using three D-type flip-flops with outputs Q_A, Q_B and Q_C, and a number of gates. Assuming that states in the state machine are encoded as Q_A:Q_B:Q_C with Q_A and Q_C being the most and least significant bits respectively. Analyze the circuit to obtain the transition table and state transition diagram.

(11 marks)

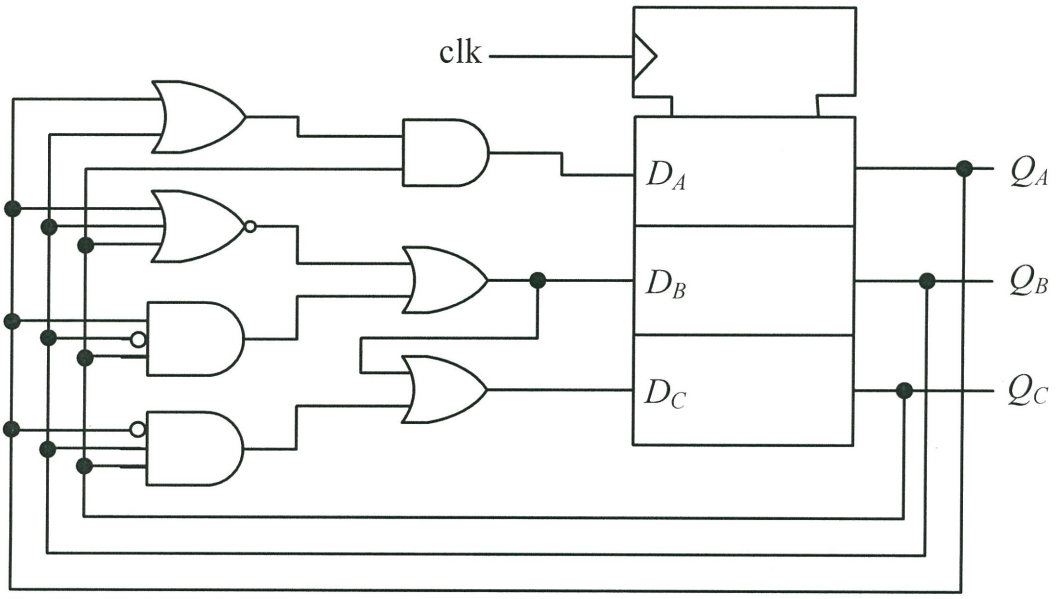

FIGURE Q3 (b)

Q4 (a) Explain briefly the demultiplexer (DEMUX) by the aid of diagram.

(4 marks)

(b) Show how 3 units of 2-to-1 demultiplexer in Figure **Q4 (b)** can be cascaded to form a 4-to-1 demultiplexer.

(5 marks)

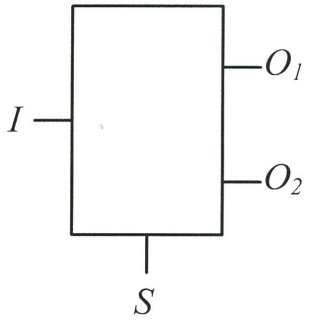

FIGURE Q4 (b)

(c) The waveforms for signals X, Y and Z shown in Figure **Q4 (c)(i)** are applied to the circuit shown in Figure **Q4 (b)(ii)**. Illustrate the waveforms for S, C and Q in the **APPENDIX II**. Assumes that initially $Q = 0$.

(6 marks)

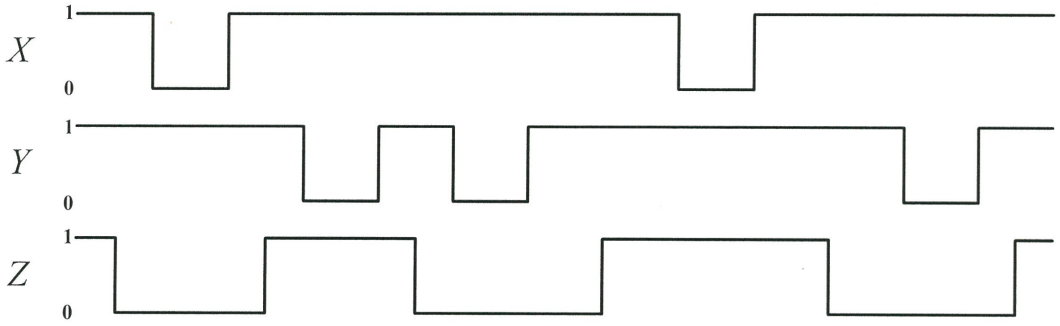

FIGURE Q4 (c)(i)

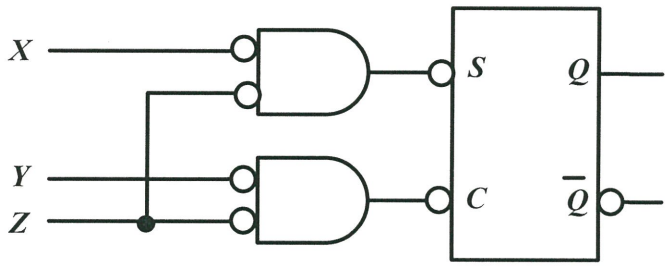

FIGURE Q4 (c)(ii)

Q5 A combinational circuit has three inputs *H*, *S*, *I* and three outputs *X*, *Y* and *Z*. Each input represents an item that a person may order at a fast food place. The items are;

- *H* stands for hot dog, which cost $3.
- *S* stands for soda, which cost $1.
- *I* stand for ice cream, which cost $2.

Each input can only be 1 or 0, which means that a customer can order each item only once (or none at all, for H=0, S=0, I=0). The outputs *X*, *Y* and *Z* represent a 3-bit encoding of the total cost of the order. For example, for H=1, S=1 and I=0 (which evaluate to $4), the output should be X=1, Y=0 and Z=0.

(a) Obtain the truth table for this combinational circuit.

(8 marks)

(b) Determine the minimum expression for *X*, *Y* and *Z* in SOP form.

(6 marks)

(c) Design the circuit using only NAND with minimum number of gates.

(6 marks)

Q6 (a) Circuit in Figure **Q6 (a)(i)** has three inputs (A, B and C) and one output (Z). Construct the truth table. Refer Figure **Q6 (a)(ii)** datasheet for pin assignment.

(8 marks)

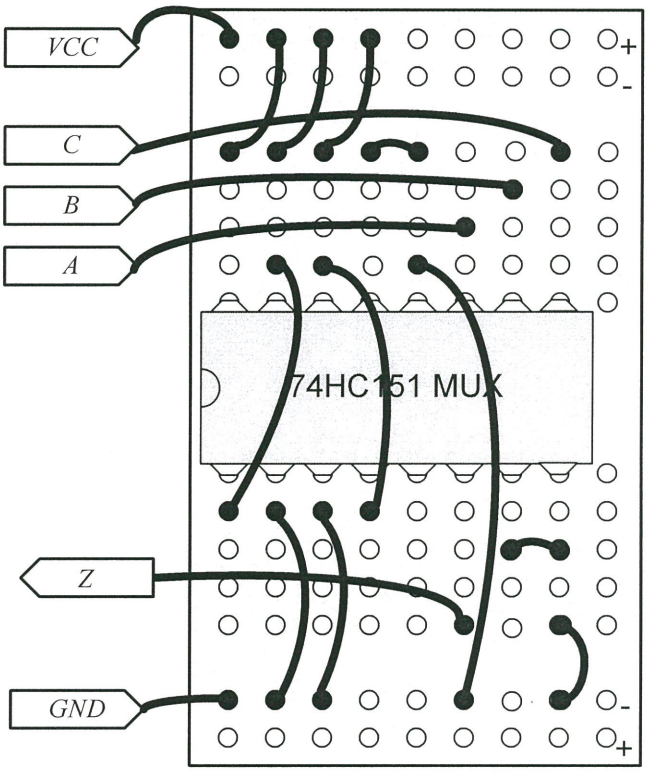

FIGURE Q6 (a)(i)

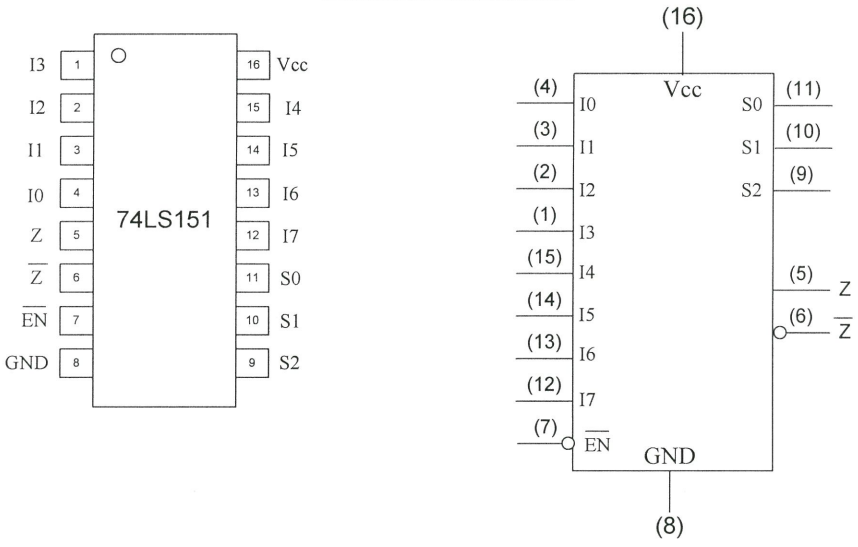

FIGURE Q6 (a)(ii)

(b) Based on truth table you obtained in **Q6(a)**, design the circuit using decoder and NAND gates in Figure **Q6 (b)(i)** (please answer in **APPENDIX III**). Show all connection. Refer to Figure **Q6 (b)(ii)** for datasheet pin assignment.

(12 marks)

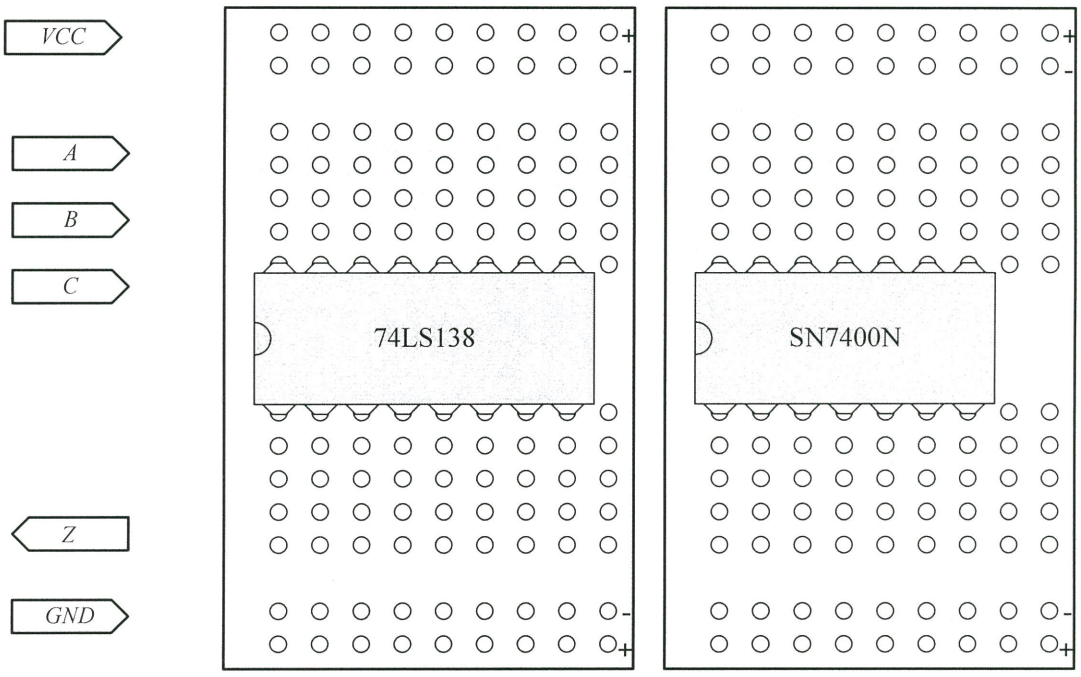

FIGURE Q6 (b)(i)

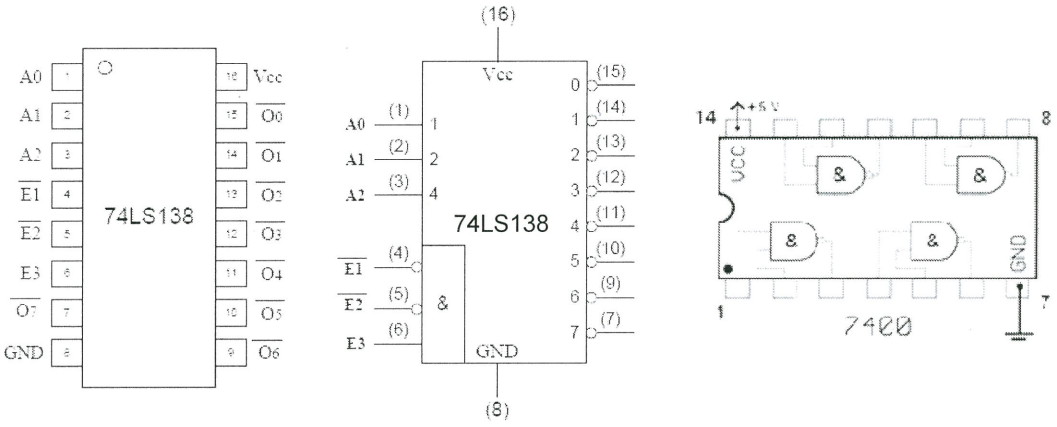

FIGURE Q6 (b)(ii)

- END OF QUESTION -

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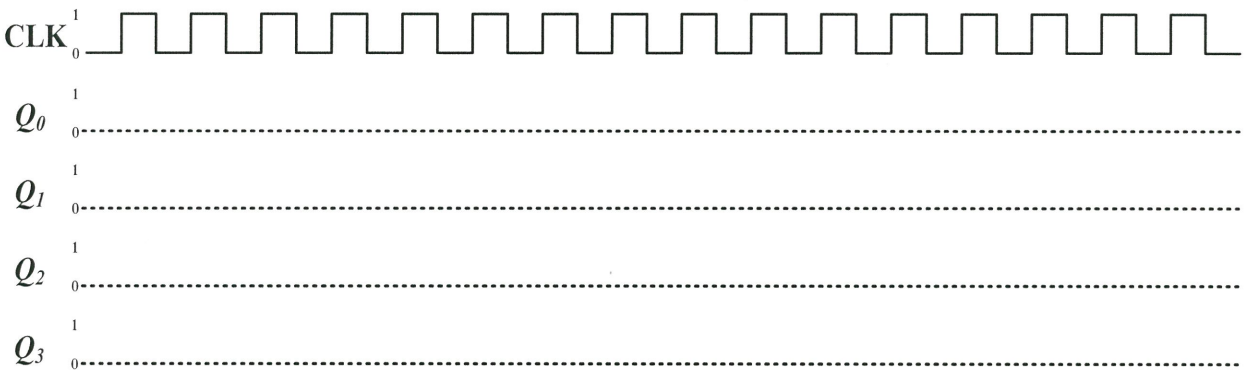
APPENDIX I



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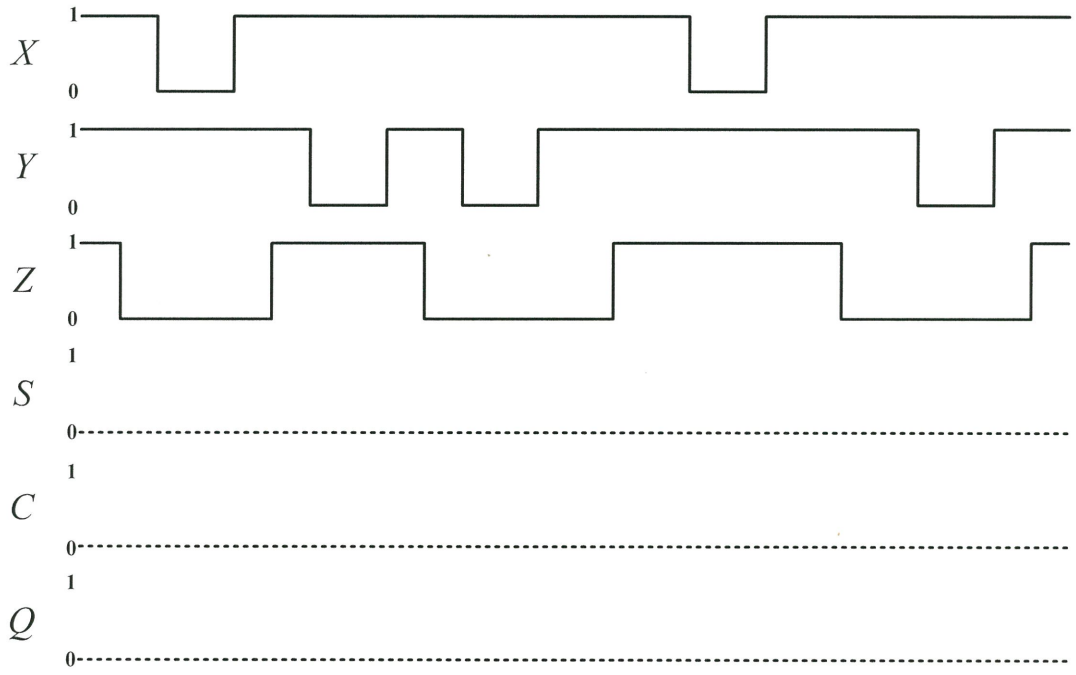
APPENDIX II



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APPENDIX III