Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JUNE 2014
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

SECTION A

Q1 _____ register keeps track of the instructions stored in program stored in memory.

(A) AR (Address Register)
(B) XR (Index Register)
(C) PC (Program Counter)
(D) AC (Accumulator)

(1 mark)

Q2 The addressing mode used in an instruction of the form ADD X Y, is

(A) absolute
(B) indirect
(C) index
(D) none of the above

(1 mark)

Q3 Cache memory acts between

(A) CPU and RAM
(B) RAM and ROM
(C) CPU and Hard Disk
(D) none of the above

(1 mark)

Q4 A Stack-organised Computer uses instruction of

(A) indirect addressing
(B) two-addressing
(C) zero addressing
(D) index addressing

(1 mark)

Q5 In a memory-mapped I/O system, which of the following will not be there?

(A) LDA
(B) IN
(C) ADD
(D) OUT

(1 mark)

Q6 The load instruction is mostly used to designate a transfer from memory to a processor register known as

(A) accumulator
(B) instruction Register
(C) program counter
(D) memory address Register

(1 mark)

Q7 The communication between the components in a microcomputer takes place via the address and

(A) I/O bus
(B) data bus
(C) address bus
(D) control lines

(1 mark)

Q8 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called

(A) relative address mode
(B) index addressing mode
(C) register mode
(D) implied mode

(1 mark)

Q9 The maximum addressing capacity of a micro processor which uses 16 bit database and 32 bit address base is

(A) 64
(B) 4 GB
(C) both (A) & (B)
(D) none of the above

(1 mark)

Q10 Status bit is also called

(A) binary bit
(B) flag bit
(C) signed bit
(D) unsigned bit

(1 mark)

SECTION B

Q1 (a) Convert the following expressions from Postfix to Infix notation.

(i) 223*5+*
(ii) 34+2034*2+-*
(iii) 534+*22212+*+*-
(iv) 12 + 3 + 4 + 5 + 6 + 7 +

(4 marks)

(b) Convert the following expressions from Infix notation to Postfix and Prefix.

(i) A/B ^ C + D × E – A × C
(ii) (B^2 – 4 × A × C) ^ (1/2)
(iii) (4 + 8) × (6 – 5) / ((3 – 2) × (2 + 2))

(6 marks)

(c) Design a program to evaluate the given arithmetic statement

$$Y = \frac{A - B + C}{G + H}$$

(i) using an accumulator.

(5 marks)

(ii) using a stack organized computer.

(5 marks)

Q2 Aircraft data bus systems allow a wide variety of avionics equipment to communicate with one another and exchange data. Bus systems can be either bidirectional or unidirectional. They can also be either serial or parallel.

(a) Explain the reason why all practical aircraft bus systems are based on serial data transfer?

(2 marks)

(b) List all lines required to interface between an input devices with input/output (I/O) interface.

(3 marks)

(c) Describe three (3) working principles of I/O interface for an input device.
(6 marks)

(d) On a synchronous bus, all devices derive timing information from a control line called the bus clock. Elaborate the processes involved by using an appropriate diagram to support your answer.
(9 marks)

Q3 (a) Pipelining is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a special dedicated segment that operates concurrently with all other segments. Illustrate a space time diagram for a six segment pipeline showing the time it takes to process eight tasks.
(7 marks)

(b) Calculate the number of clock cycles that it takes to process 200 tasks in Q3(a).
(4 marks)

(c) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10 ns.

(i) Analyse the speedup ratio of the pipeline for 100 tasks.
(2 marks)

(ii) Analyse the maximum speed up that can be achieved.
(2 marks)

Q4 (a) Fetching an instruction and loading it into the IR is usually referred to as the instruction fetch phase. Whilst performing the operation specified in the instruction constitutes the instruction execution phase. List five (5) step sequences of actions via these phases to perform an instruction.
(5 marks)

(b) Identify the differences between hardwired and micro-programmed control unit for the following attributes:
(i) speed
(ii) cost of implementation
(iii) flexibility
(iv) ability to handle complex instructions
(v) instruction set size
(5 marks)

(c) With the aid of a diagram, generate the arithmetic instruction execution in the sequence of control steps intended for single bus architecture for the instruction of ADD R1, (R2).

(11 marks)

Q5 (a) A computer system has a 4KB SRAM cache memory. Plan two (2) solutions to improve cache hit and cache latency.

(4 marks)

(b) For any given application running on a computer system with several levels of caches, set up two (2) techniques on how to increase the cache efficiency such that the overall computer performance can be increased?

(4 marks)

(c) Assuming that a computer system has the following memory properties:

Main memory:

Number of address lines: 15 bits
Number of input/output (data) lines: 32 bits

Cache memory:

Number of address lines: 10 bits
Number of input/output (data) lines: 32 bits
Number of words per block: 8

Based on the above specifications, determine the total number of bits for tag, block and word in the following scheme:

(i) direct mapping scheme

(3 marks)

(ii) associative mapping scheme

(3 marks)

- END OF QUESTIONS -