Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME	:	ANALOG ELECTRONICS
COURSE CODE	:	BEL 10203
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JUNE 2014
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **THIRTEEN (13)** PAGES

Q1 (a) Describe and differentiate the processes that result in a bonding structure as illustrated in Figure **Q1(a)(i)** and **Q1(a)(ii)**. Hence determine the result of each process.

(5 marks)

(b) The circuit in Figure **Q1(b)** is a centre-tapped rectifier. Referring to this circuit;

(i) Summarize the operation of a centre-tapped rectifier.

(4 marks)

(ii) Draw and label the input, V_i and output waveforms V_{out} if Switch S1 and Switch S2 are closed but Switch S3 is opened.

(4 marks)

(iii) Draw and label the output waveforms V_{out} if all switches are closed.

(2 marks)

(c) Design a clamper circuit to perform the function indicated in Figure **Q1(c)**. Prove your design with calculation.

(5 marks)

(d) Figure **Q1(d)** shows the Zener regulation circuit. V_{in} is 40 V, R_1 is 50 Ω, R_L is 100 Ω and the breakdown voltage of the zener diode is 20 V. Find:

(i) the voltage drop across the load resistance R_L,

(1 mark)

(ii) the current through the load resistor R_L,

(1 mark)

(iii) the voltage drop across R_1,

(1 mark)

(iv) the current through R_1,

(1 mark)

(v) the current through the zener diode.

(1 mark)

Q2 Figure **Q2** shows a common emitter amplifier which is to be manufactured using transistors with a nominal β value of 200.

(a) Determine the collector bias current when $\beta = 200$, taking into account the base current of the transistor.

(3 marks)

(b) Evaluate the collector bias current in the cases $\beta = 150$ and $\beta = 250$. Conclude the results.

(3 marks)

(c) Draw a small-signal equivalent circuit of the amplifier and hence prove that the voltage gain may be written as:

$$\frac{-R_C}{re+R_E}$$

You may neglect the transistor's small-signal output resistance, r_o.

(4 marks)

(d) Evaluate the expression given in **Q2(c)** by assuming $\beta = 200$.

(4 marks)

(e) Determine the voltage gain of the amplifier if the emitter resistor, R_E were bypassed using a capacitor?

(2 marks)

(f) If the amplifier in Figure **Q2** has an applied load, R_L of 4.7 kΩ, a source resistance, R_S of 1.5 kΩ, an input capacitor, C_S of 1 μF, an output capacitor, C_C of 1 μF and an emitter capacitor, C_E of 100 μF;

(i) Draw its AC equivalent circuit for low frequency response.

(2 marks)

(ii) Determine the low cutoff frequencies f_{LS}, f_{LC} and f_{LE}.

(6 marks)

(iii) State the dominant frequency, f_L and sketch the frequency response.

(1 mark)

Q3 A Field Effect Transistor (FET) circuit has a MATLAB plot of the transfer characteristics curve and the bias line as in Figure **Q3**. Based on the specifications given as follows:

$$V_{DD} = 15 \text{ V}, V_{DS} = 5.475 \text{ V and } I_1 = I_2 = \frac{V_{DD}}{R_1 + R_2} = 16.67\ \mu A;$$

(a) Design the circuit (with bypass capacitor). Hence determine the value of all resistors.

(12 marks)

(b) Draw the AC equivalent of the circuit and calculate its input impedance Z_i, output impedance Z_o and voltage gain A_v. Assume $r_d \geq 10R_D$.

(8 marks)

Q4 (a) For the BJT cascade amplifier of Figure **Q4(a)**,

(i) calculate the emitter current I_E, for each stage.

(2 marks)

(ii) draw the AC equivalent circuit.

(3 marks)

(iii) calculate the voltage gain of each stage and the overall AC voltage gain.

(5 marks)

(b) For the Darlington network of Figure **Q4(b)**,

(i) determine the DC bias voltages, V_{B1}, V_C, and V_{E2} and currents, I_{B1} and I_{E2}.

(5 marks)

(ii) draw the AC equivalent circuit, then calculate the mid-band voltage gain, $A_v = V_o/V_i$.

(5 marks)

Q5 Figure **Q5** shows the class-B power amplifier circuit. Given that Rb1 = Rb2 = 3.9kΩ, supply voltage, ±Vcc = ±20V, Rload =10Ω, Ri = 47Ω and Cin = 1 μF. For this figure:

(a) Explain the circuit operation.

(4 marks)

(b) Draw the maximum peak output voltage, $V_{op(max)}$ across the Rload.

(2 marks)

(c) Calculate the circuit efficiency if the peak output voltage, V_{op} across the Rload is 10V.

(4 marks)

- END OF QUESTION –

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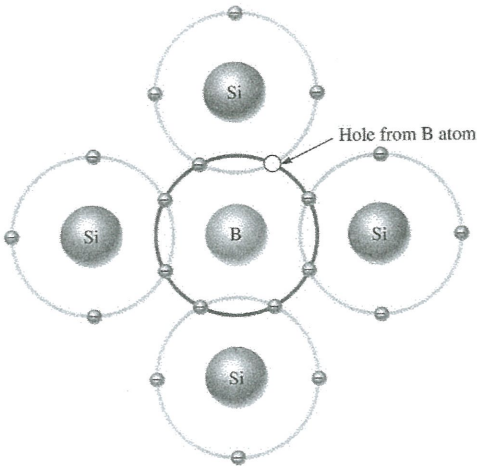

FIGURE Q1(a)(i)

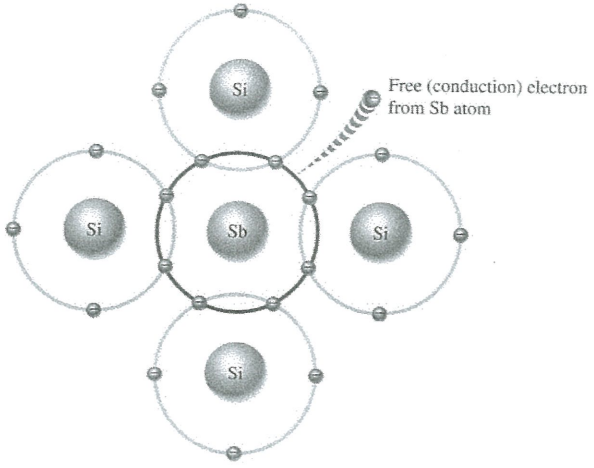

FIGURE Q1(a)(ii)

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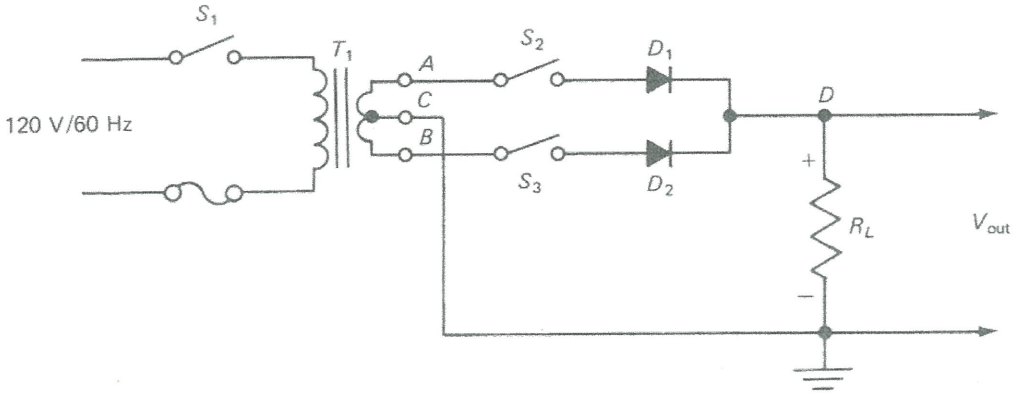

FIGURE Q1(b)

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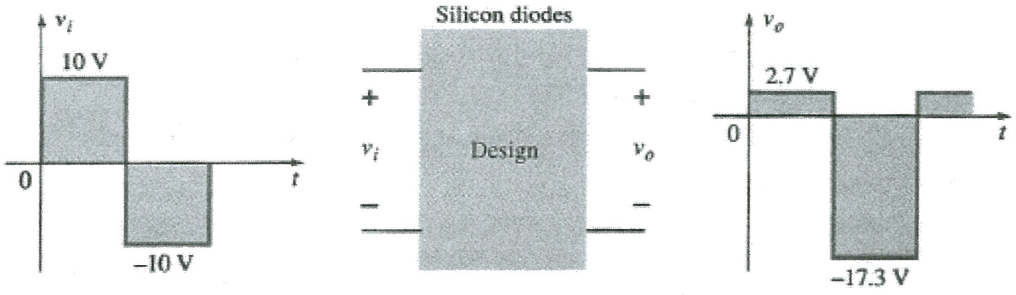

FIGURE Q1(c)

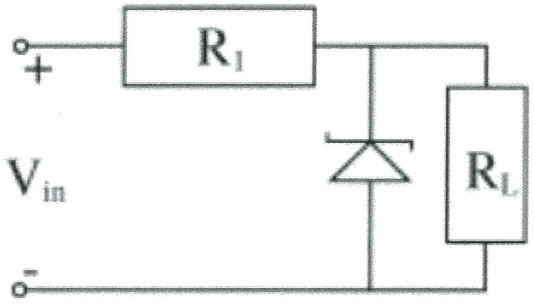

FIGURE Q1(d)

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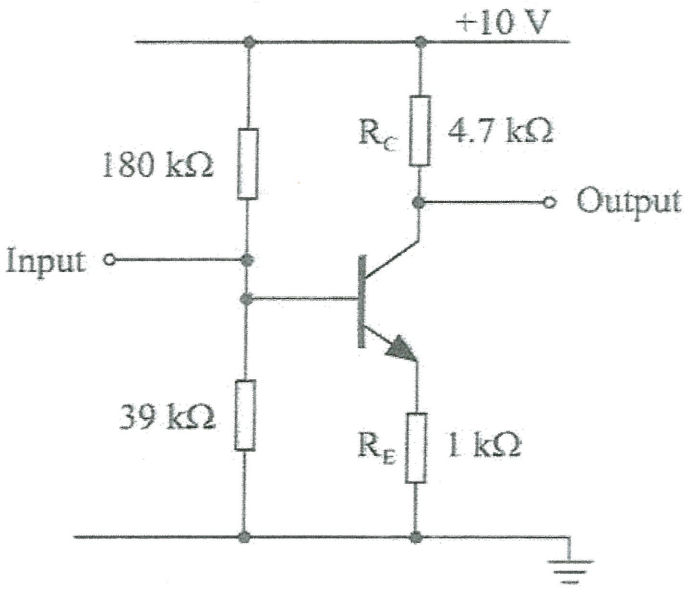

FIGURE Q2

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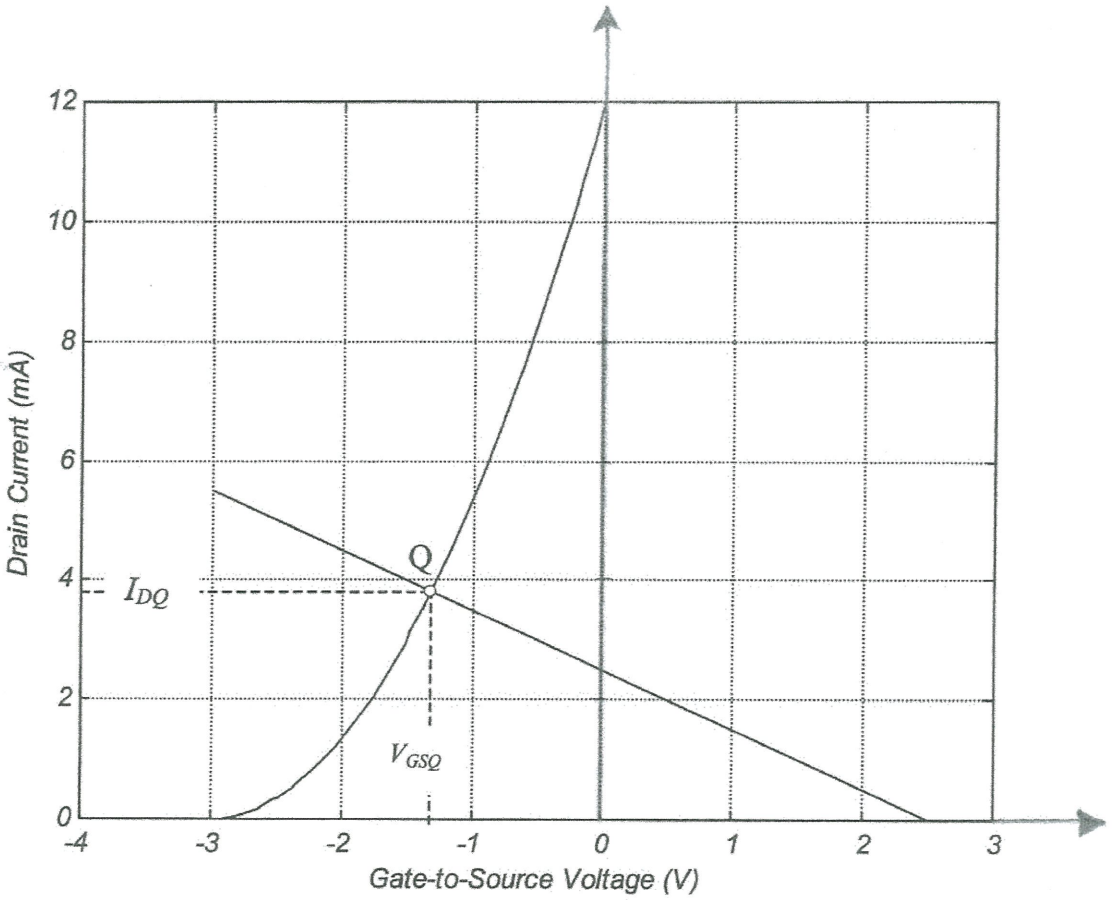

FIGURE Q3

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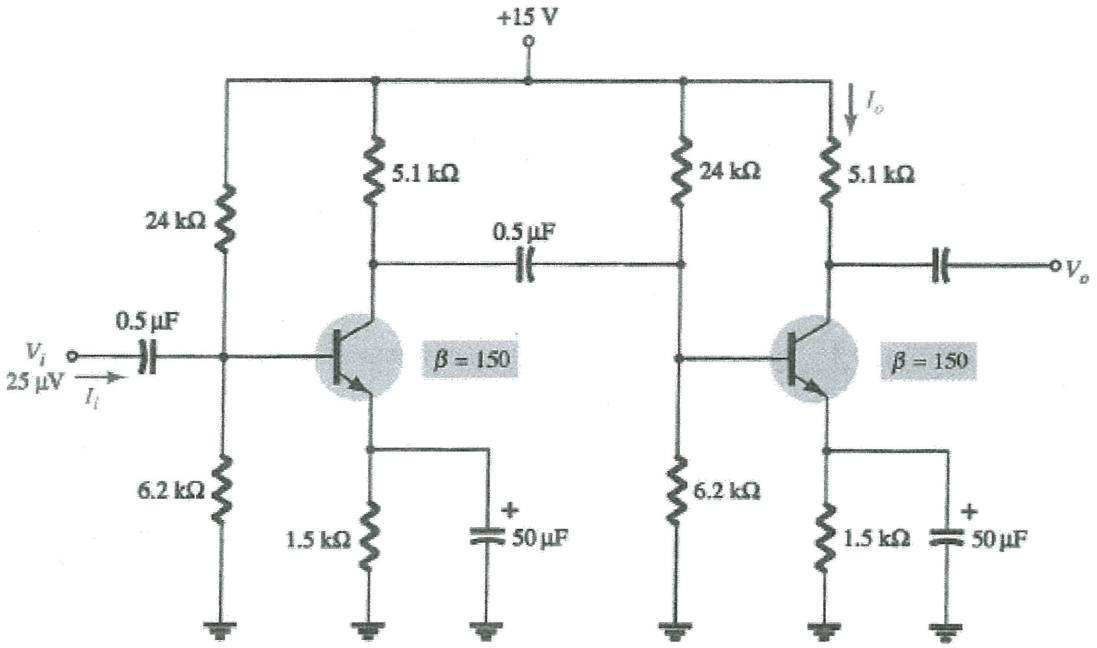

FIGURE Q4(a)

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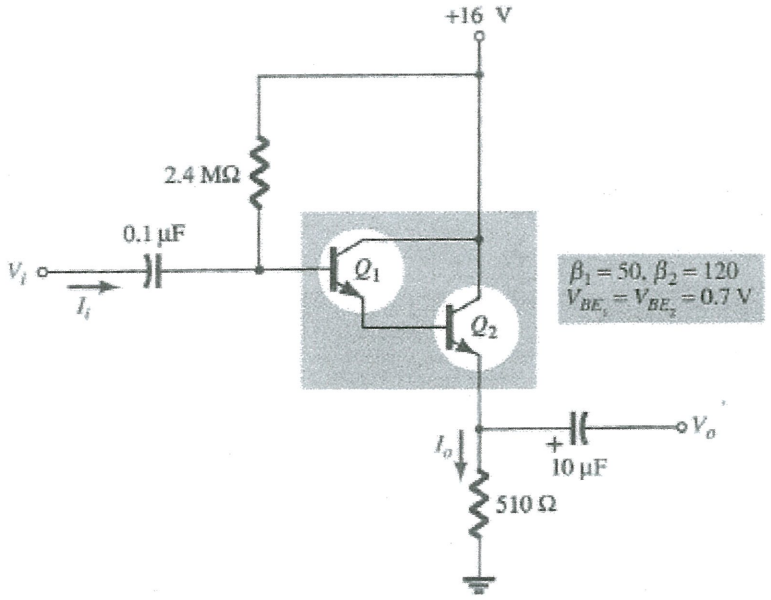

FIGURE Q4(b)

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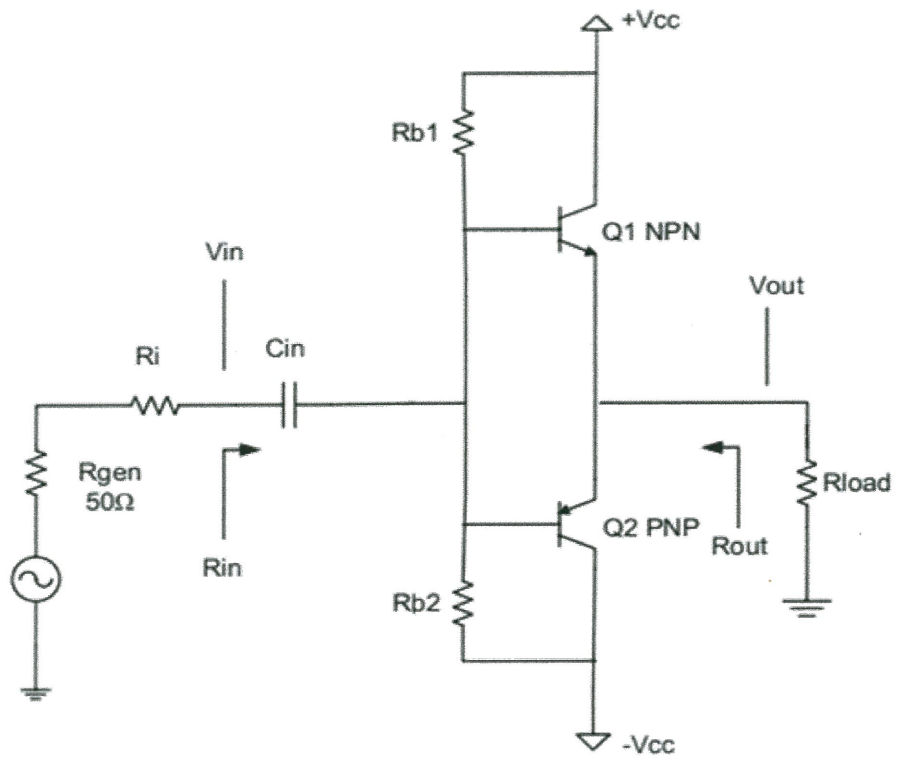

FIGURE Q5