UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2013/2014

COURSE NAME : ADVANCED SEMICONDUCTOR DEVICES

COURSE CODE : BED 41003

PROGRAMME : BEJ

EXAMINATION DATE : JUNE 2014

DURATION : 3 HOURS

INSTRUCTION :
1. ANSWER **ALL** QUESTIONS IN SECTION A
2. ANSWER ANY **TWO** **(2)** QUESTIONS IN SECTION B

THIS QUESTION PAPER CONSISTS OF **NINE** (**9**) PAGES

SECTION A

Q1 (a) Explain **ONE (1)** main characteristic of a power MOSFET structure that supports its purpose as a power device.

(3 marks)

(b) Formation of an ohmic contact in a metal-semiconductor junction would lead to two possibilities; an ideal non-rectifying barrier or a tunneling barrier.

(i) Point out **TWO (2)** characteristics of ohmic contact that made it as a non-rectifying barrier.

(6 marks)

(ii) Solve the ohmic barrier height at room temperature when the contact resistance is quadruple the thermal voltage. Given the effective Richardson constant, $A^* = 114$ A/(K-cm)^2.

(5 marks)

(iii) Predict the effect in ohmic contact when the junction compound is forward biased, that is metal is more positive than semiconductor.

(6 marks)

Q2 (a) In general, an IMPATT diode employs both impact ionisation and avalanche mechanisms in its operation.

(i) Identify **ONE (1)** drawback of IMPATT diode due to employment of the specified mechanisms.

(3 marks)

(ii) Solve the breakdown voltage for a GaAs one-sided IMPATT diode with doping concentration of 3 x 10^{17} cm^{-3} using diode characteristic in Figure **Q2(a)(ii)**.

(6 marks)

(iii) Referring to Figure **Q2(a)(iii)**, analyse the reason the electrical field decreases uniformly in *n*-region of one-sided IMPATT diode.

(6 marks)

(b) Figure **Q2(b)** shows the energy band diagram of a resonant tunnelling (RT) diode. Referring to this diagram, explain **TWO (2)** reasons RT diode requires band discontinuity at both conduction and valence bands.

(5 marks)

Q3 (a) In resonant tunnelling diode structure, layers of well and barrier are sandwiched between two highly-doped semiconductor materials. Analyse the reason both well and barrier layers are formed using undoped semiconductor materials.

(4 marks)

(b) In an n-type Si JFET, the parameters are given as follows:

$$N_a = 3 \times 10^{18}\ cm^{-3},\ N_d = 8 \times 10^{16}\ cm^{-3},\ a = 0.5\ \mu m,\ V_{bi} = 0.896V$$

(i) Solve the internal pinch-off voltage, V_{p0}.

(3 marks)

(ii) Solve the required gate voltage, V_G, so that the undepleted channel is 0.20 μm.

(7 marks)

(c) Figure **Q3(c)** shows the breakdown voltage, V_{BR}, in thyristor with respect to doping concentration, N_{n1}.

(i) Analyse the reason the avalanche breakdown likely to occur at large n_1-layer width, W_{n1}.

(3 marks)

(ii) Analyse the reason the avalanche breakdown likely to occur at high N_{n1}.

(3 marks)

SECTION B

Q4 (a) An anisotype heterojunction is formed between n-type AlAs and p-type GaAs. Assume that the process takes place at room temperature and zero external bias.

(i) Formulate the expression of N_{GaAs} in term of N_{AlAs}, so that the depletion width of AlAs equals 0.01 times depletion width of GaAs.

(7 marks)

(ii) Formulate the expression of N_{GaAs} in term of N_{AlAs} to limit the junction capacitance not exceeds 1 μF. Given the built-in potential is 1.20 V.

(8 marks)

(b) Figure **Q4(b)** shows the structure of thyristor in reverse biased condition.

(i) Analyse why punch through is likely to cause junction breakdown when depletion width equals W_{n1}.

(3 marks)

(ii) Deduce the major effect when junction breakdown occurs in thyristor.

(2 marks)

Q5 (a) A MESFET uses Al as its gate electrode and *n*-type Ge as the epitaxial layer. Figure **Q5(a)** shows its I_D-V_D characteristic for various V_G values.

(i) Formulate the minimum required thickness of epitaxial layer, a, in term of its doping concentration, N_D, to achieve saturation drain voltage, V_{Dsat} not less than 1.2 V.

(6 marks)

(ii) Predict the effect of saturated drain voltage, V_{Dsat}, if the epitaxial layer is changed to *n*-type GaAs. Given the MESFET operates at $V_G = 0$. Use the appropriate formula to aid the explanation.

(9 marks)

(b) Ballistic motion is one of the hot electron device characteristics that refers to high speed carrier flow in semiconductor material.

(i) Analyse the importance of this characteristic in semiconductor devices.

(3 marks)

(ii) Deduce the effect on the carriers if they are exposed to ballistic motion for a long time.

(2 marks)

Q6 (a) The structure of a Read IMPATT diode and its corresponding doping profile is shown in Figure **Q6(a)**.

(i) Predict the new doping profile if the intrinsic region of Read diode is changed to become a lightly doped *n*-type region. Use diagram to aid the explanation.

(8 marks)

(ii) Formulate the minimum required electric field, E_{min}, in Si Read diode in term of doping concentration of *n*-type and intrinsic regions (N_1 and N_2). Given the width of *n*-type and intrinsic regions are 0.4 μm and 12.5 μm respectively, and E_m is 10^4 V/cm.

(7 marks)

(b) Figure **Q6(b)** shows the structure of a MODFET that used AlGaAs and GaAs as its substrate.

(i) Analyse the reason its channel is formed in undoped GaAs layer.

(3 marks)

(ii) Deduce the effect on pinch off voltage if the concentration in doped AlGaAs layer is increased.

(2 marks)

- END OF QUESTION -

FINAL EXAMINATION

SEMESTER/SESSION	: SEM II / 2013/2014	PROGRAMME	: BEJ
COURSE NAME	: ADVANCED SEMICONDUCTOR DEVICES	COURSE CODE	: BED 41003

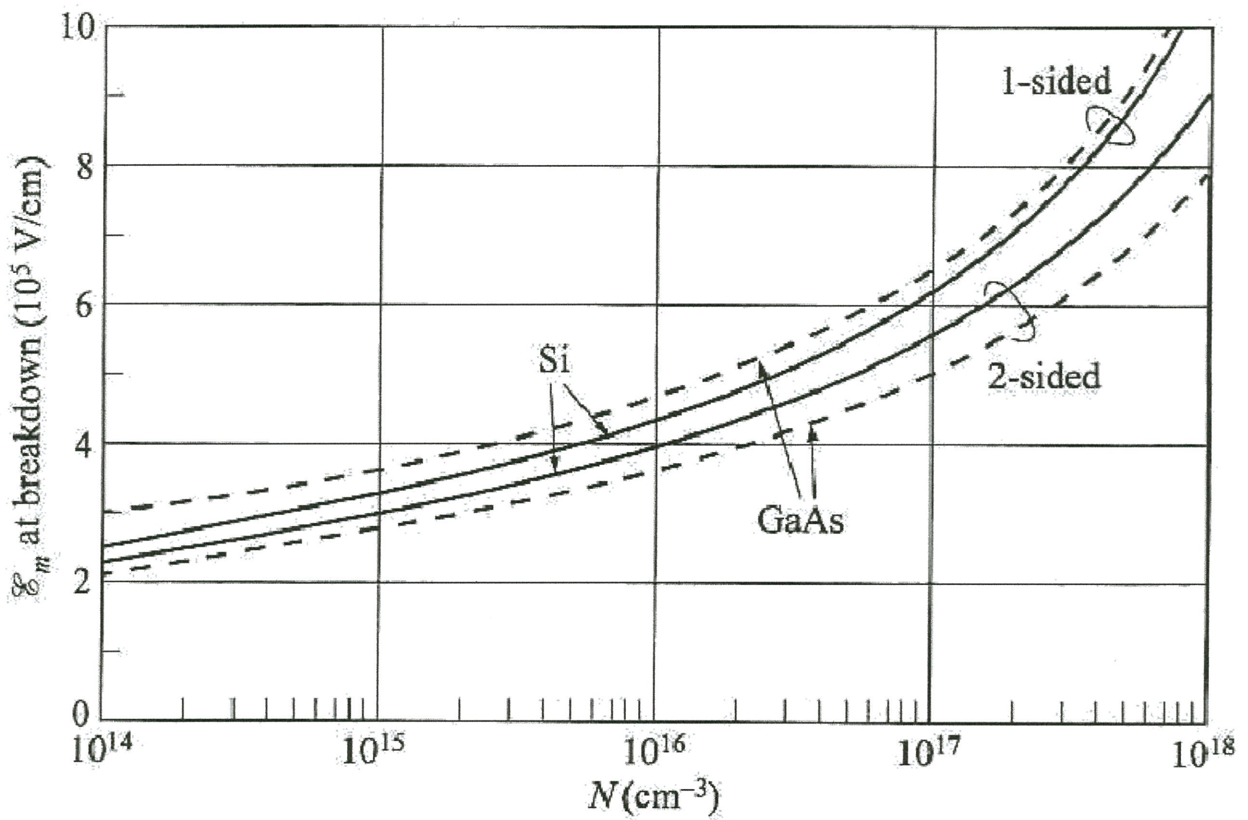

FIGURE Q2(a)(ii)

FINAL EXAMINATION

SEMESTER/SESSION	: SEM II / 2013/2014	PROGRAMME	: BEJ
COURSE NAME	: ADVANCED SEMICONDUCTOR DEVICES	COURSE CODE	: BED 41003

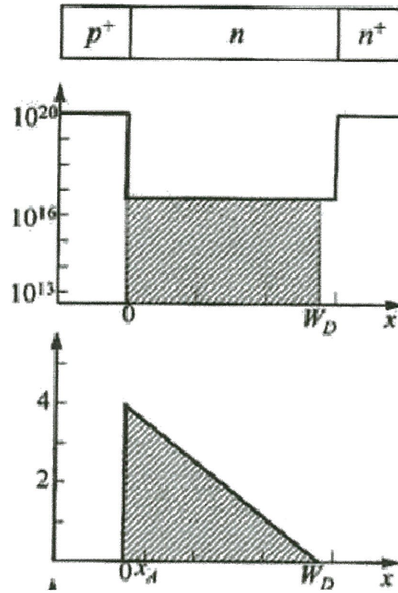

FIGURE Q2(a)(iii)

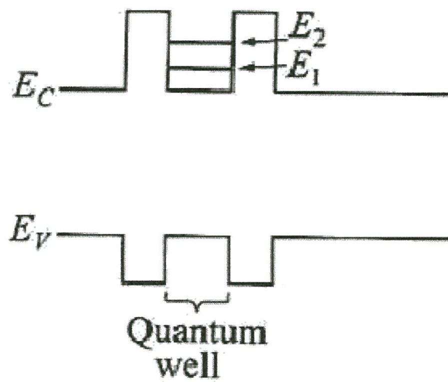

FIGURE Q2(b)

FINAL EXAMINATION

SEMESTER/SESSION : SEM II / 2013/2014
COURSE NAME : ADVANCED SEMICONDUCTOR DEVICES
PROGRAMME : BEJ
COURSE CODE : BED 41003

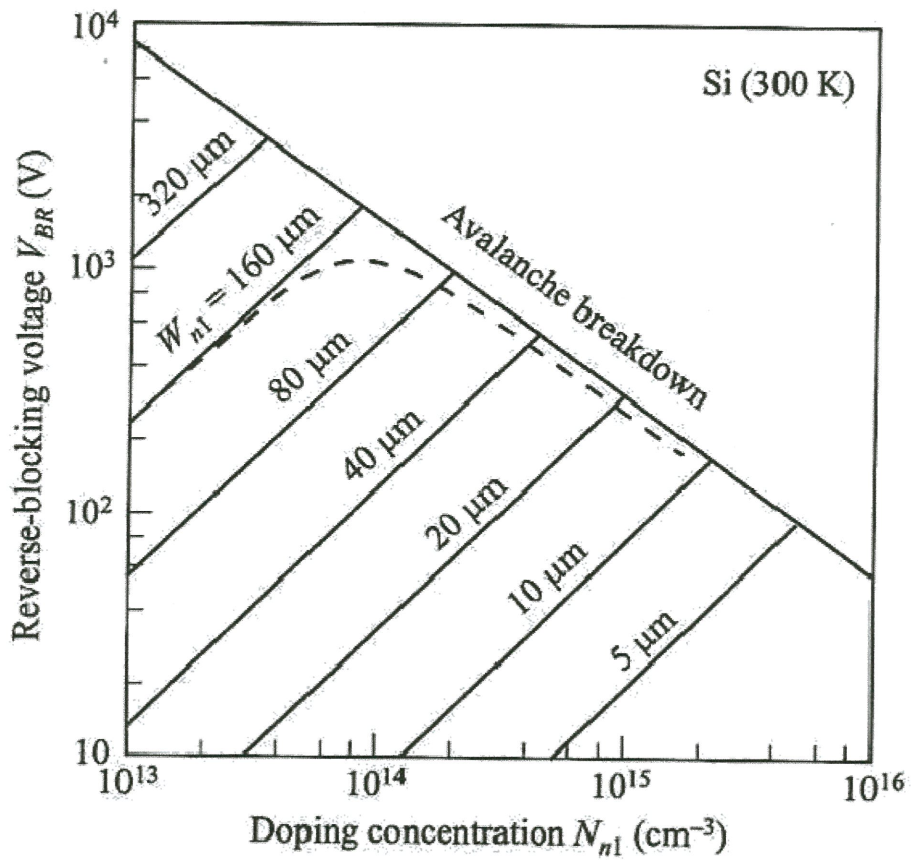

FIGURE Q3(c)

FINAL EXAMINATION

SEMESTER/SESSION : SEM II / 2013/2014
COURSE NAME : ADVANCED SEMICONDUCTOR DEVICES
PROGRAMME : BEJ
COURSE CODE : BED 41003

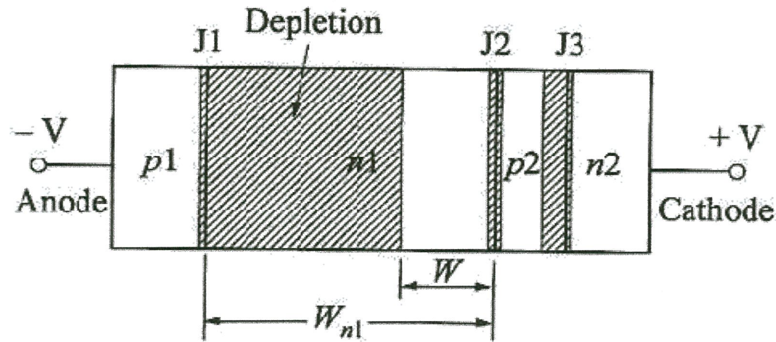

FIGURE Q4(b)

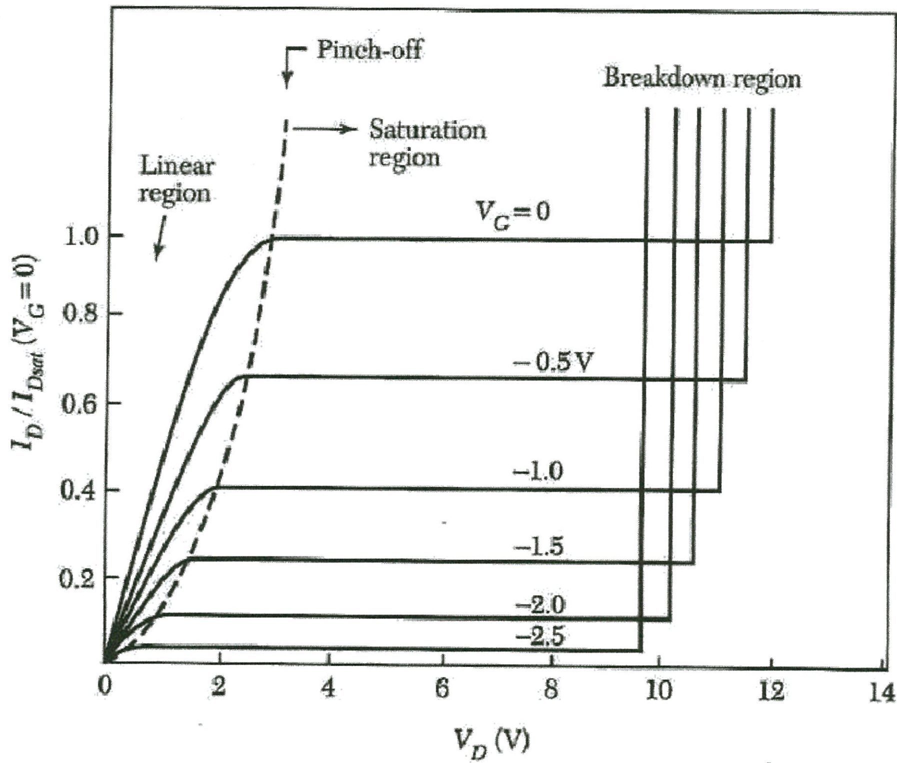

FIGURE Q5(a)

FINAL EXAMINATION

SEMESTER/SESSION : SEM II / 2013/2014
COURSE NAME : ADVANCED SEMICONDUCTOR DEVICES
PROGRAMME : BEJ
COURSE CODE : BED 41003

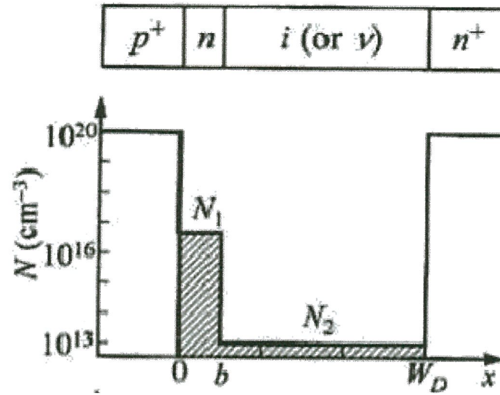

FIGURE Q6(a)

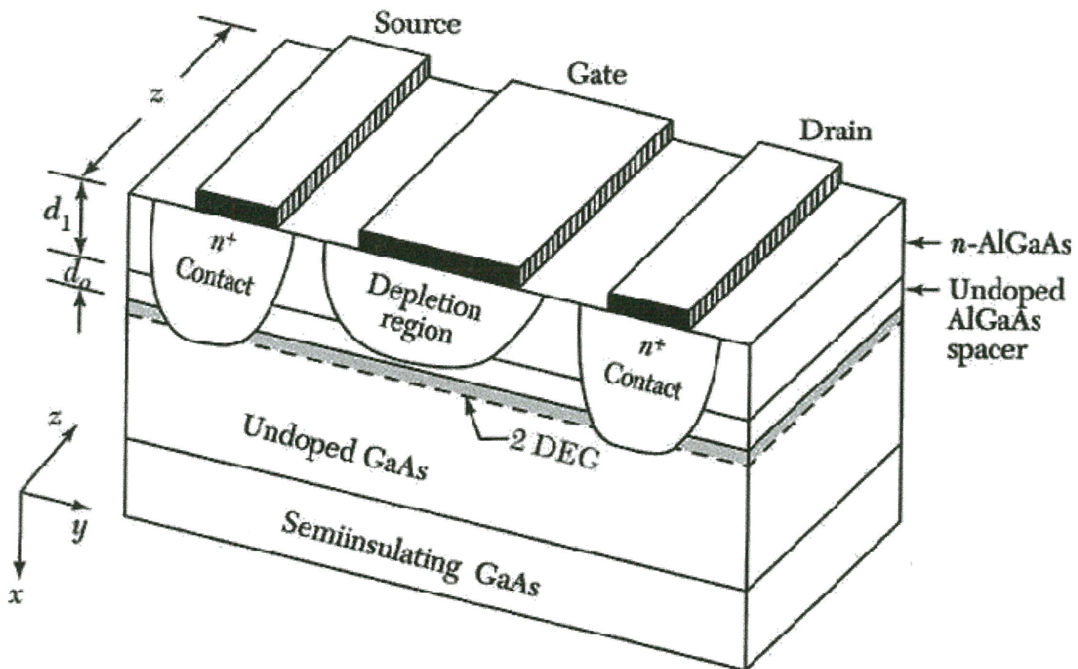

FIGURE Q6(b)