UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2010/2011

COURSE	:	MICROPROCESSOR AND MICROCONTROLLER
COURSE CODE	:	BEE 3233
PROGRAMME	:	BACHELOR OF ELECTRICAL ENGINEERING WITH HONOURS
EXAMINATION DATE	:	APRIL/MAY 2011
DURATION	:	3 HOURS
INSTRUCTIONS	:	ANSWER **ALL** QUESTIONS IN PART A AND ANY **TWO (2)** QUESTIONS IN PART B

THIS QUESTION PAPER CONSISTS OF TWENTY THREE (23) PAGES

PART A

Q1 (a) Figure Q1 shows the data logger system that uses PIC16C71 as an interface between the sensor and the computer. The PIC will read the analog signal from the sensor, convert the analog signal to digital signal before send it to the computer via the RS232 cable.

    (i) Determine and explain the initialization value of ADCON0 and ADCON1 in special function register if the PIC is clocked at 4MHz.

(6 marks)

    (ii) Write a sequence of instructions to read the converted value (in ADRES) to the RAM of the PIC.

(2 marks)

    (iii) For the data transmission, calculate the duration of the stop bit, T if the speed of the transmission is 9600 baud.

(1 mark)

    (iv) Write a delay subroutine to obtain a speed of 9600 baud and show how to use that delay routine to send logic low for duration of one (1) bit.

(8 marks)

    (v) Design an algorithm to send the data from the PIC to the computer by using a flowchart. Given the transmission speed is 9600 baud, start bit = '0' and stop bit = '1'.

(8 marks)

(b) Write a sequence of instructions to enable the interrupt on RB0 of PIC16F84A. The interrupt must be detected on every rising edge of the signal on RB0.

(4 marks)

Q2 (a) Status Register (SR) of MC68000 microprocessor can be divided into two sections which are system byte and user byte.

   (i) Determine the value of flag bit C and Z if the SR contains $150A.

   (2 marks)

   (ii) Write an instruction that will set bit X of CCR by using a logic instruction (AND/OR/EOR).

   (3 marks)

(b) Explain the error for each of the following MC 68000 instructions:

   (i) MOVE.W   #$28E00, D5
   (ii) ANDI.B   D3, #7
   (iii) EOR.L   D1, A1

   (6 marks)

(c) Write a routine that will perform the control program as per algorithm specified as follows:

   WHILE M > N
   DO N++

   (5 marks)

(d) Figure Q2(d) shows the MC 68000 assembly program written in EASY68K simulation software.

   (i) After the program is assembled, what is the first address of the program and the data respectively?

   (2 marks)

   (ii) After the program is executed, write the value of the 16 bits data in Table 2(d) for the given address.

   (5 marks)

   (iii) After the program is executed, what is the value of data for D0 and D1?

   (2 marks)

PART B

Q3 (a) Interrupt is one of the important features in all modern computers. Explain the execution of the interrupt in PIC16F84A and list all the interrupt sources for the PIC16F84A.

(6 marks)

(b) Write a sequence of instructions to enable the interrupt on RB0 of PIC16F84A. The interrupt must be detected on every rising edge of the signal on RB0.

(4 marks)

(c) Figure Q3(c) shows the schematic of the PIC application that will count every eight (8) pulses that applied to RA4 to determine a number of full axis turn of the motor. When the number of full axis turn reach 255, the PIC will save the value of TMR0 in RAM location 1CH. Write a full program to implement the application as per specified.

(10 marks)

(d) Calculate the pre-load value required in TMR0 to obtain a delay of 1ms when the timer is overflow. Given the clock rate is 4MHz and the pre-scale ratio selected is 8:1.

(5 marks)

Q4 (a) Explain the differences between subroutine and macro.

(6 marks)

(b) Design a flowchart base on the subroutine as follows:

```
MyRoutine
            MOVLW    d'100'
            MOVWF    TEMP
Loop
            MOVLW    d'5'
            SUBWF    TEMP
            MOVLW    d'10'
            SUBWF    TEMP,W
            BTFSS    STATUS,Z
            GOTO     Loop
            RETURN
```

(8 marks)

(c) Figure Q4(c) shows a simple set of traffic lights. Write a program to light the R (R1 and R2), Y (Y1 and Y2) and G (G1 and G2) LEDs based on the truth table in Table Q4(c).

(11 marks)

Q5   (a)   (i) Design a memory address decoder for the MC 68000 with a ROM of 16k word (32 byte) starts from $000000, RAM consist 64k word (128 byte) starts from $400000 and I/O which range from $800000 to $80001F.

(17 marks)

(b)   Write a 68000 assembly program to divide a 16-bit signed number in the high word of D1 by an 8-bit signed number in the lowest byte of D1.

(8 marks)

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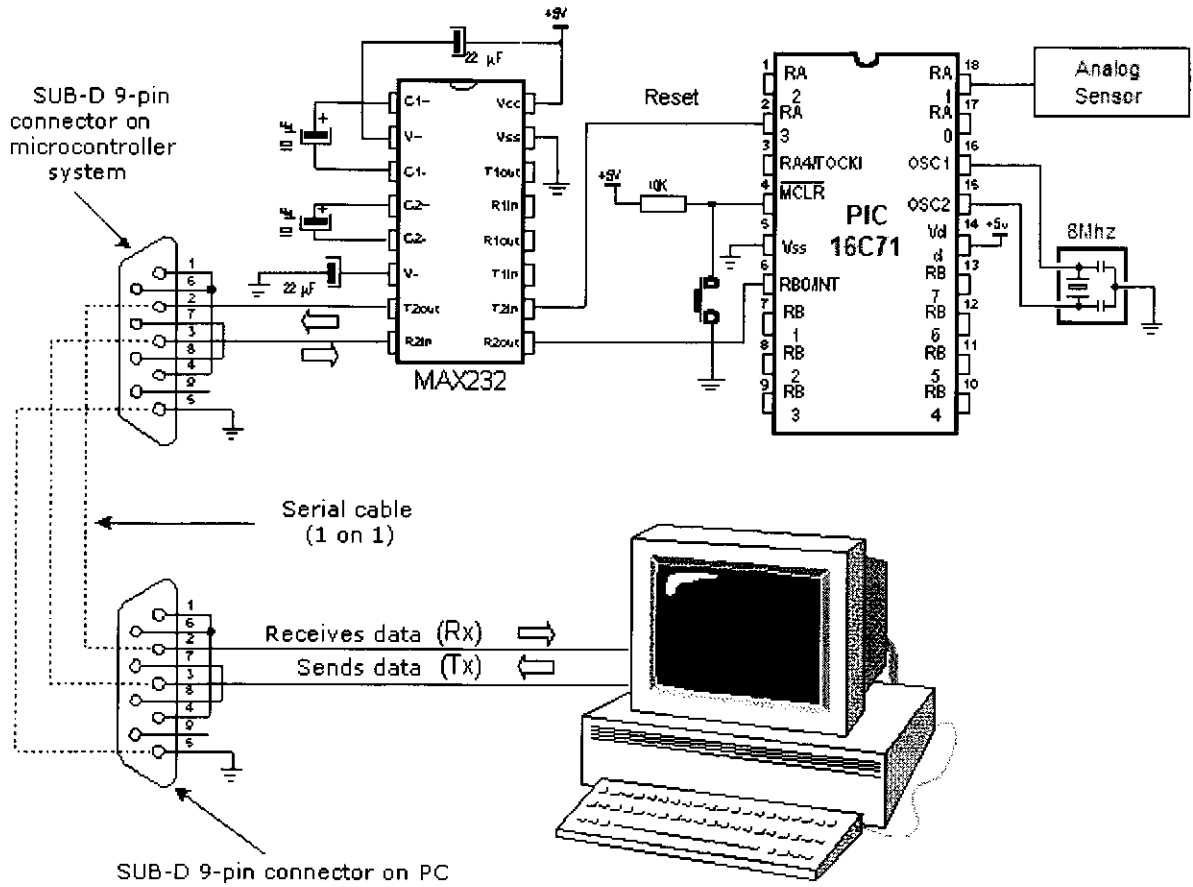
Figure Q1

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                    MICROCONTROLLER

```
CODE      EQU      $1000
DATA      EQU      $2000

          ORG      CODE
PROG      MOVE.L   NUMBERS, D0
          MOVE.L   NUMBERS+4, D1
AGAIN     ROL.B    #1, D1
          SUBQ.W   #1, D0
          MOVE.W   D0, SUM
          BNE      AGAIN
          TRAP     #15



          ORG      DATA
NUMBERS   DC.L     $4
          DC.L     1200
SUM       DC.W     0
          END      PROG
```

Figure Q2(d)

Address	2000	2002	2004	2006	2008
Content					

Table Q2(d)

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Figure Q3(c)

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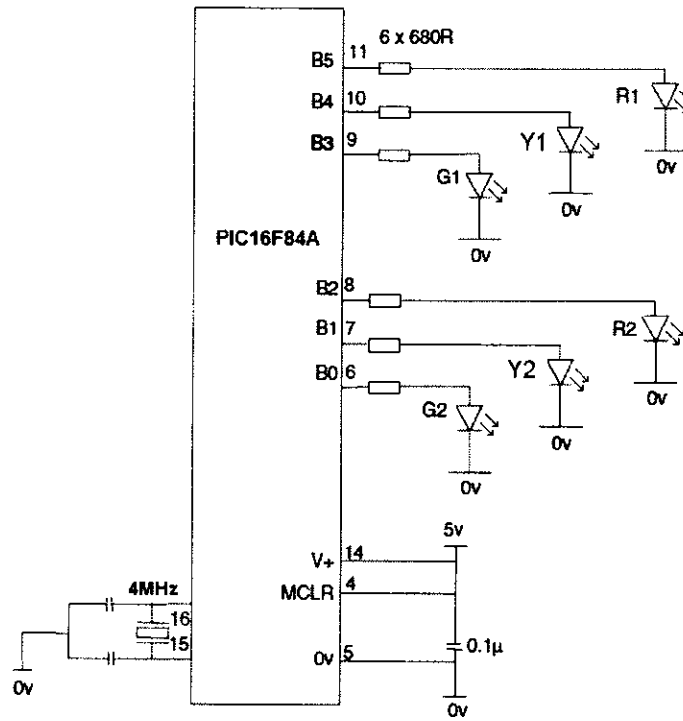
Figure Q4(c)

Time	B7	B6	B5	B4	B3	B2	B1	B0
			R1	Y1	G1	R2	Y2	G2
3sec	0	0	1	0	0	1	0	0
3sec	0	0	1	1	0	1	0	0
6sec	0	0	0	0	1	1	0	0
3sec	0	0	0	1	0	1	0	0
3sec	0	0	1	0	0	1	0	0
3 sec	0	0	1	0	0	1	1	0
5 sec	0	0	1	0	0	0	0	1
3 sec	0	0	1	0	0	0	1	0
REPEAT								

Table Q4(c)

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Special Function Register (SFR) File Summary for PIC16F84A

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- ----	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS[2]	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA[4]	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB[5]	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC[1]					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- ----	11
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS [2]	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	16
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC[1]					---0 0000	11
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition
Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.
2: The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ status bits in the STATUS register are not affected by a $\overline{\text{MCLR}}$ Reset.
3: Other (non power-up) RESETS include: external RESET through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.
4: On any device RESET, these pins are configured as inputs.
5: This is the value that will be in the port output latch.
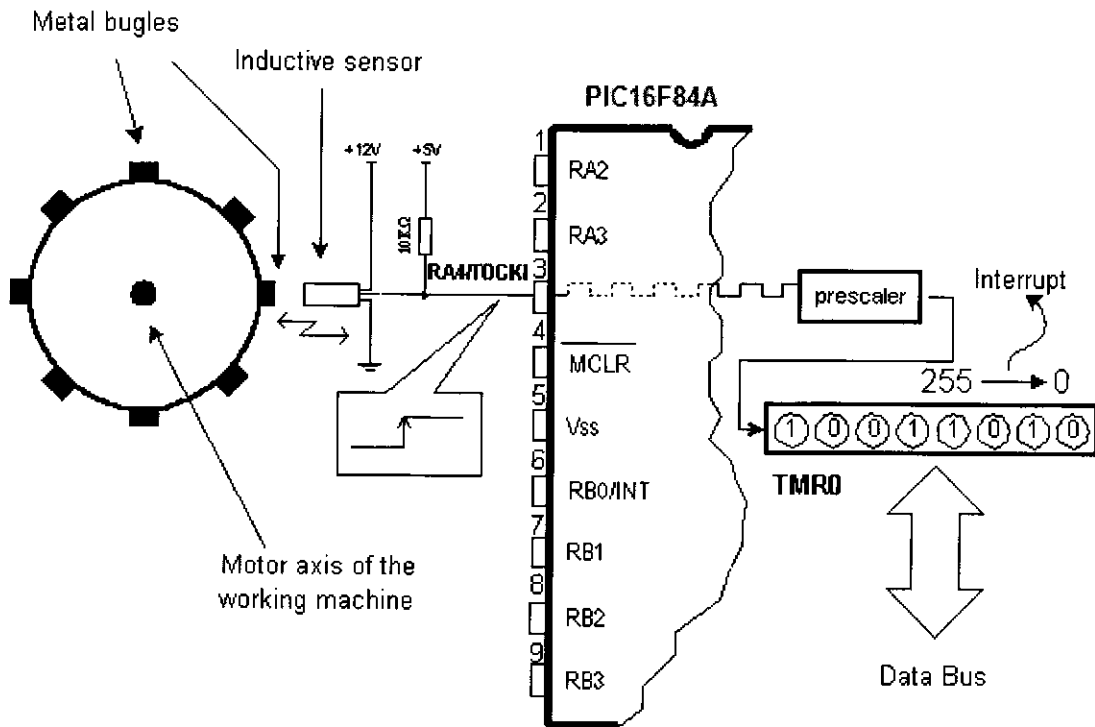
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STATUS Register of PIC16F84A

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

bit 7   bit 0

bit 7-6   **Unimplemented:** Maintain as 'o'

bit 5   **RP0**: Register Bank Select bits (used for direct addressing)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

bit 4 $\overline{TO}$: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 $\overline{PD}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2   **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1   **DC**: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0   **C**: Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

    Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

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OPTION Register of PIC16F84A / PIC16C71

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

bit 7   bit 0

bit 7   **RBPU**: PORTB Pull-up Enable bit
             1 = PORTB pull-ups are disabled
             0 = PORTB pull-ups are enabled by individual port latch values

bit 6   **INTEDG**: Interrupt Edge Select bit
             1 = Interrupt on rising edge of RB0/INT pin
             0 = Interrupt on falling edge of RB0/INT pin

bit 5   **T0CS**: TMR0 Clock Source Select bit
             1 = Transition on RA4/T0CKI pin
             0 = Internal instruction cycle clock (CLKOUT)

bit 4   **T0SE**: TMR0 Source Edge Select bit
             1 = Increment on high-to-low transition on RA4/T0CKI pin
             0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3   **PSA**: Prescaler Assignment bit
             1 = Prescaler is assigned to the WDT
             0 = Prescaler is assigned to the Timer0 module

bit 2-0   **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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INTCON Register of PIC16F84A

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF

bit 7   bit 0

bit 7   **GIE:** Global Interrupt Enable bit

1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6   **EEIE:** EE Write Complete Interrupt Enable bit

1 = Enables the EE Write Complete interrupts
0 = Disables the EE Write Complete interrupt

bit 5   **T0IE:** TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4   **INTE:** RB0/INT External Interrupt Enable bit

1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3   **RBIE:** RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2   **T0IF:** TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1   **INTF:** RB0/INT External Interrupt Flag bit

1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0   **RBIF:** RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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Special Function Register (SFR) File Summary for PIC16C71

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (1)
Bank 0											
00h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(3)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(3)	STATUS	IRP(5)	RP1(5)	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
04h(3)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					---x 0000	---u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	ADCON0	ADCS1	ADCS0	(6)	CHS1	CHS0	GO/DONE	ADIF	ADON	00-0 0000	00-0 0000
09h(3)	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
0Ah(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(3)	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(3)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(3)	STATUS	IRP(5)	RP1(5)	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
84h(3)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
86h	TRISB	PORTB Data Direction Control Register								1111 1111	1111 1111
87h(4)	PCON	—	—	—	—	—	—	POR	BOR	---- --qq	---- --uu
88h	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00
89h(3)	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
8Ah(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(3)	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.
2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
3: These registers can be addressed from either bank.
4: The PCON register is not physically implemented in the PIC16C71, read as '0'.
5: The IRP and RP1 bits are reserved on the PIC16C710/71/711, always maintain these bits clear.
6: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

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STATUS Register of PIC16C71

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

bit7   bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit,
    read as '0'
- n = Value at POR reset

bit 7: **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5: **RP1:RP0:** Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4: **$\overline{TO}$:** Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$:** Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2: **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C:** Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

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INTCON Register of PIC16C71

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF

bit7   bit0

```
R = Readable bit
W = Writable bit
U = Unimplemented bit,
     read as '0'
- n = Value at POR reset
```

bit 7: **GIE:**[1] Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables A/D interrupt
0 = Disables A/D interrupt

bit 5: **TOIE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **TOIF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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ADCON0 Register of PIC16C71

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	(1)	CHS1	CHS0	GO/DONE	ADIF	ADON

bit7   bit0

R = Readable bit
W = Writable bit
U = Unimplemented
   bit, read as '0'
- n = Value at POR reset

bit 7-6:   **ADCS1:ADCS0:** A/D Conversion Clock Select bits
           00 = Fosc/2
           01 = Fosc/8
           10 = Fosc/32
           11 = FRc (clock derived from an RC oscillation)

bit 5:   **Unimplemented:** Read as '0'.

bit 4-3:   **CHS1:CHS0:** Analog Channel Select bits
           00 = channel 0, (RA0/AN0)
           01 = channel 1, (RA1/AN1)
           10 = channel 2, (RA2/AN2)
           11 = channel 3, (RA3/AN3)

bit 2:   **GO/DONE:** A/D Conversion Status bit

           If ADON = 1:
           1 = A/D conversion in progress (setting this bit starts the A/D conversion)
           0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1:   **ADIF:** A/D Conversion Complete Interrupt Flag bit
           1 = conversion is complete (must be cleared in software)
           0 = conversion is not complete

bit 0:   **ADON:** A/D On bit
           1 = A/D converter module is operating
           0 = A/D converter module is shutoff and consumes no operating current

Note 1: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

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ADCON1 Register of PIC16C71

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PCFG1	PCFG0

bit7   bit0
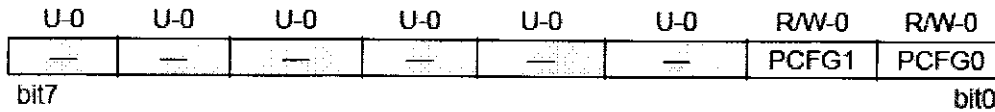
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1-0: **PCFG1:PCFG0**: A/D Port Configuration Control bits

PCFG1:PCFG0	RA1 & RA0	RA2	RA3	VREF
00	A	A	A	V_{DD}
01	A	A	VREF	RA3
10	A	D	D	V_{DD}
11	D	D	D	V_{DD}

A = Analog input

D = Digital I/O

FINAL EXAMINATION

SEMESTER/SESSION : II/2010/2011   PROGRAM : 3 BEE
COURSE   : MICROPROCESSOR AND   COURSE CODE : BEE 3233
                MICROCONTROLLER

PIC16F84A Instruction Set Summary

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO},\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO},\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

FINAL EXAMINATION

SEMESTER/SESSION : II/2010/2011   PROGRAM : 3 BEE
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                    MICROCONTROLLER

Data Transfer Instruction MC68000

Mnemonic	Meaning	Type	Operand Size	Operations
MOVE	Move	MOVE EAs, EAd	8, 16, 32	(EAs) → EAd
		MOVE EA,CCR	8	(EA) → CCR
		MOVE EA,SR	16	(EA) → SR
		MOVE SR, EA	16	SR → EA
		MOVE USP,An	32	USP → An
		MOVE An,USP	32	An → USP
		MOVEA EA,An	16, 32	(EA) → An
		MOVEQ #XXX,Dn	8	#XXX → Dn
MOVEM	Move multiple	MOVEM Reg_list,EA	16, 32	Reg_list → EA
		MOVEM EA,Reg_list	16, 32	(EA) → Reg_list
LEA	Load effective address	LEA EA,An	32	EA → An
EXG	Exchange Swap	EXG Rx,Ry	32	Rx ↔ Ry
SWAP	Clear	SWAP Dn	16	$Dn31{:}16 \leftrightarrow Dn15{:}0$
CLR		CLR EA	8, 16, 32	0 → EA

FINAL EXAMINATION

SEMESTER/SESSION : II/2010/2011   PROGRAM : 3 BEE
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                  MICROCONTROLLER

Compare and Test MC68000 Instruction

Mnemonic	Meaning	Type	Operand Size	Operation
CMP	Compare	CMP EA,Dn	8, 16, 32	N, Z, V, C
		CMPA EA,An	16, 32	N, Z, V, C
		CMPI #XXX,EA	8, 16, 32	N, Z, V, C
		CMPM (Ay)$^+$,(AY)$^+$	8, 16, 32	N, Z, V, C
TST	Test	TST EA	8, 16, 32	N, Z, V, C

Logical MC68000 Instruction
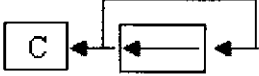
Mnemonic	Meaning	Type	Operand Size	Operation
AND	Logical AND	AND EA,Dn	8, 16, 32	$(EA) \cdot Dn \to Dn$
		AND Dn,EA	8, 16, 32	$Dn \cdot (EA) \to EA$
		ANDI #XXX,EA	8, 16, 32	$\#XXX \cdot (EA) \to EA$
		ANDI #XXX,CCR	8	$\#XXX \cdot CCR \to CCR$
		ANDI #XXX,SR	16	$\#XXX \cdot SR \to SR$
OR	Logical OR	OR EA,Dn	8, 16, 32	$(EA) + Dn \to Dn$
		OR Dn,EA	8, 16, 32	$Dn + (EA) \to EA$
		ORI #XXX,EA	8, 16, 32	$\#XXX + (EA) \to EA$
		ORI #XXX,CCR	8	$\#XXX + CCR \to CCR$
		ORI #XXX,SR	16	$\#XXX + SR \to SR$
EOR	Logical exclusive-OR	EOR Dn,EA	8, 16, 32	$Dn \oplus (EA) \to EA$
		EORI #XXX,EA	8, 16, 32	$\#XXX \oplus (EA) \to EA$
		EORI #XXX,CCR	8	$\#XXX \oplus CCR \to CCR$
		EORI #XXX,SR	16	$\#XXX \oplus SR \to SR$
NOT	Logical NOT	NOT EA	8, 16, 32	$(\overline{EA}) \to EA$

FINAL EXAMINATION

SEMESTER/SESSION : II/2010/2011
COURSE : MICROPROCESSOR AND
MICROCONTROLLER

PROGRAM : 3 BEE
COURSE CODE : BEE 3233

Rotate MC68000 Instruction

Mnemonic	Meaning	Type	Operand Size	Operation
ROL	Rotate left	ROL #XXX,Dy ROL Dx,Dy ROL EA	8, 16, 32 8, 16, 32 8, 16, 32	
ROR	Rotate right	ROR #XXX,Dy ROR Dx,Dy ROR EA	8, 16, 32 8, 16, 32 8, 16, 32	
ROXL	Rotate left through extend	ROXL #XXX,Dy ROXL Dx,Dy ROXL EA	8, 16, 32 8, 16, 32 8, 16, 32	
ROXR	Rotate right through extend	ROXR #XXX,Dy ROXR Dx,Dy ROXR EA	8, 16, 32 8, 16, 32 8, 16, 32	

Bit Manipulation MC68000 Instruction

Mnemonic	Meaning	Type	Operand Size	Operation
BTST	Test a bit	BTST #XXX,EA BTST Dn,EA	8, 32 8, 32	$\overline{EA}$ bit $\rightarrow$ Z
BSET	Test a bit and set	BSET #XXX,EA BSET Dn,EA	8, 32 8, 32	$\overline{EA}$ bit $\rightarrow$ Z 1 $\rightarrow$ EA bit
BCLR	Test a bit and clear	BCLR #XXX,EA BCLR Dn,EA	8, 32 8, 32	$\overline{EA}$ bit $\rightarrow$ Z 0 $\rightarrow$ EA bit
BCHG	Test a bit and change	BCHG #XXX,EA BCHG Dn,EA	8, 32 8, 32	$\overline{EA}$ bit $\rightarrow$ Z $\overline{EA}$ bit $\rightarrow$ EA bit

FINAL EXAMINATION

SEMESTER/SESSION : II/2010/2011   PROGRAM : 3 BEE
COURSE   : MICROPROCESSOR AND   COURSE CODE : BEE 3233
                   MICROCONTROLLER

Bcc Instruction

Instruction	Meaning	Arithmetic	If the test is true
BEQ	EQual to zero	U	$Z=1$
BNE	Not Equal to zero	U	$Z=0$
BMI	Minus	U	$N=1$
BPL	Plus	U	$N=0$
BCS/LO	Carry Set/LOwer	U	$C=1$
BCC/HS	Carry Clear/Higher or Same	U	$C=0$
BVS	oVerflow Set	S	$V=1$
BVC	oVerflow Clear	S	$V=0$
BGT	GreaTer than	S	$Z+(N\oplus V)=0$
BLT	Less Than	S	$N\oplus V=1$
BGE	Greater than or Equal	S	$N\oplus V=0$
BLE	Less than or Equal	S	$Z+(N\oplus V)=0$
BHI	Higher	U	$C+Z=0$
BLS	Lower than or Same	U	$C+Z=1$

			Marks			**Summary**	
Q1	a	Comprehension	3	12		Knowledge	0
		Analysis	3	12		Comprehension	16
	b	Synthesize	2	8		Analysis	36
	c	Comprehension	1	4		Synthesize	48
	d	Analysis	4	16		Evaluation	0
		Synthesize	4	16		**Total**	**100**
	e	Analysis	2	8			
		Synthesize	6	24			
		Total	25	25			

			Marks			**Summary**	
Q2	a	Analysis	4	16		Knowledge	0
		Analysis	2	8		Comprehension	0
		Synthesize	4	16		Analysis	84
	b	Analysis	15	60		Synthesize	16
	c	Analyisis	0	0		Evaluation	0
		Synthesize	0	0		**Total**	**100**
	d	Analyisis	0	0			
		Synthesize	0	0			
		Total	25	25			

			Marks			**Summary**	
Q3	a	Knowledge	2	8		Knowledge	8
		Comprehension	4	16		Comprehension	16
	b	Analyisis	1	4		Analysis	28
		Synthesize	3	12		Synthesize	48
	c	Analyisis	4	16		Evaluation	0
		Synthesize	6	24		**Total**	**100**
	d	Analyisis	2	8			
		Synthesize	3	12			
		Total	25	25			

			Marks			**Summary**	
Q4	a	Knowledge	6	24		Knowledge	24
	b	Analysis	3	12		Comprehension	44
		Synthesize	5	20		Analysis	12
	c	Comprehension	11	44		Synthesize	20
		Total	25	100		Evaluation	0
						Total	**100**

			Marks			**Summary**	
Q5	a	Comprehension	6	24		Knowledge	20
		Analysis	6	24		Comprehension	44
		Knowledge	5	20		Analysis	24
	b	Comprehension	5	20		Synthesize	12
		Synthesize	3	12		Evaluation	0
		Total	25	100		**Total**	**100**