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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2010/2011**

COURSE : DIGITAL SYSTEMS DESIGN

COURSE CODE : BEX 31503/BEE 3133

**PROGRAMME : BACHELOR OF ELECTRICAL
ENGINEERING WITH HONOURS**

EXAMINATION DATE : APRIL/MAY 2011

DURATION : THREE (3) HOURS

**INSTRUCTIONS : ANSWER ALL QUESTIONS IN
PART A AND ANY TWO (2)
QUESTIONS IN PART B**

THIS QUESTION PAPER CONSISTS OF TEN (10) PAGES

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PART A: QUESTION 01 – 05 (70 marks)

- Q1 (a)** The trend of complementary metal oxide semiconductor (CMOS) technology improvement continues to be driven by the need to integrate more functions within a given silicon area as depicted in Figure Q1(a). As an example, the 32-nm CMOS technology enables designs with multi-core processors, parallel digital signal processors (DSPs), field programmable gate arrays (FPGAs), embedded random access memory (eRAM), as well as wireless communication capabilities in a single chip. Discuss three (3) point of view related with the trend shown as well as the validity of Moore's law that has been outlined in 1965.

(6 marks)

- (b)** Explain the following terms. Use an appropriate diagram to support your explanations.

(i) Design rules.

(2 marks)

(ii) Top-down and bottom-up design approaches.

(4 marks)

- (c)** In your circuit design, two major problems have been identified: high power consumption and interconnect delay. As project leader for a group of an application specific integrated circuit (ASIC) engineer, what solutions would you suggest to solve these problems?

(3 marks)

- Q2** (a) Electronic components in automotive are now essential for various functions such as to control movements, to maintain chemical, mechanical, and electrical processes, to provide entertainment and communication and also to ensure safety. As an electronic system engineer in automotive company, you are responsible to verify both main electronic switches of m and n that are connected to catalytic converter module as illustrated in Figure Q2(a). The catalytic converter will be activated if both functions, m and n are equal. Do you agree that $m = n$?

(8 marks)

- (b) (i) Using the Quine-McCluskey tabulation method, simplify the following Boolean function.

$$T = f(a, b, c, d)$$

$$T = \sum_m (0, 1, 2, 3, 8, 9, 11, 13, 15)$$

$$D = \sum_m (10, 14)$$

Where D = Don't cares condition.

(5 marks)

- (ii) Sketch the transistor-level schematic circuit for the simplified function in Q2(b)(i).

(4 marks)

- Q3** (a) Based on the design specification given in Figure Q3(a), what conclusions can be made to relate with the very large scale integration (VLSI) designer philosophy?

(5 marks)

- (b) In field programmable gate array (FPGA) design and implementation, the FPGA compiler returns a timing error if the propagation delay between any two registers exceeds the FPGA clock period. Propagation delay time, low-to-high-level output (t_{LH}) can be defined as time needed for the output arise from the 10% V_{DD} to 90% V_{DD} . Prove that $t_{LH} = 2.2R_pC_{out}$.

(5 marks)

Q4 (a) Answer TRUE or FALSE.

(i) All VHDL files require an entity declaration and an architecture body.

(1 mark)

(ii) The architecture body indicates the input and output ports of the VHDL design.

(1 mark)

(iii) A port in VHDL is a connection from a VHDL design entity to the outside world.

(1 mark)

(iv) The VHDL language was originally developed by the Institute of Electrical Engineers (IEE) committee as a standardised language for describing hardware.

(1 mark)

(v) `our_component` is a valid name for any entity in a VHDL design.

(1 mark)

(b) As a team member for computational mathematic design unit in your company, you are to design a full subtractor circuit that computes $A - B - C$, where C is the borrow from the next less significant digit and produces a difference, D , and a borrow from the next more significant bit, P .

(i) Formulate the truth table for your subtractor circuit.

(4 marks)

(ii) Implement your subtractor circuit using only NAND gates with two inputs.

(4 marks)

(iii) Write the VHDL code that implements your subtractor circuit.

(4 marks)

- Q5** (a) Consider the cross-section profile shown in Figure Q5(a). Sketch the top view of the device and label all the important regions.

(5 marks)

- (b) Identify the logic expression implemented by the stick diagram shown in Figure Q5(b).

(6 marks)

PART B: QUESTION 06 – 09 (30 marks)

Q6 (a) Consider the following transistor-level schematic shown in Figure Q6(a). Identify the Boolean equation that describes the circuit function.

(6 marks)

(b) Consider the following function.

$$g = x \cdot \overline{(y \cdot z + z \cdot w)}$$

(i) Construct the transistor-level schematic circuit using the minimum number of transistors.

(4 marks)

(ii) Sketch the Euler path and stick diagram based on the answer in Q6(b)(i).

(5 marks)

Q7 (a) Write a VHDL code for a three-input NAND gate with an inertial delay of 5 ns.

(4 marks)

(b) Write an entity description and three architecture models of a 3-to-8 decoder using the following methods.

(i) Boolean operators.

(3 marks)

(ii) **when . . . else** statement.

(4 marks)

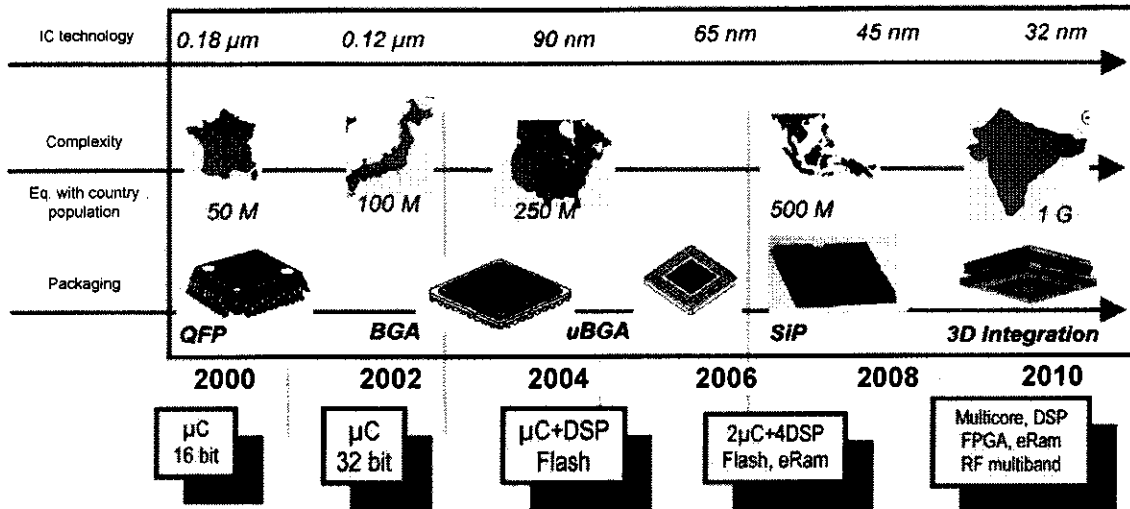
(iii) **with . . . select** statement.

(4 marks)

- Q8** (a) Explain the difference between a Mealy machine and a Moore machine.
(6 marks)
- (b) A state machine has two inputs A, B and one output, Z . If the sequence of the input pairs: $A=1 B=1, A=1 B=0, A=0 B=0$ is detected, Z become 1, during the final cycle of the sequence, otherwise the output remains at 0. Sketch the state transition diagram and construct the state table for the state machine.
(9marks)
- Q9** (a) (i) What is the difference in between structural and functional testing?
(4 marks)
- (ii) What assumptions are made by the single-stuck-fault model?
(2 marks)
- (b) Consider the circuit shown in Figure Q9(b).
- (i) Derive tests for $A/1$ and $A/0$, and determine which other faults these test cover.
(6 marks)
- (ii) Show that it is not possible to derive a test for $G/0$.
(3 marks)

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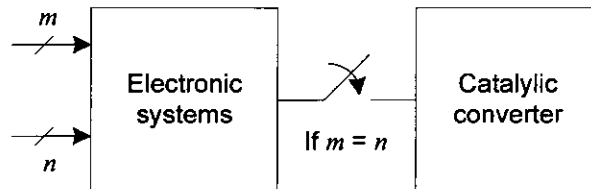
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Source:

S. M. Aziz, E. Sicard, and S. B. Dhia, Effective Teaching of the Physical Design of Integrated Circuits using Educational Tools, *IEEE Transactions on Education*, Vol. 53, No. 4, November 2010, pp. 517 - 531

FIGURE Q1(a)



$$m = x_1 x_2' x_5' + x_1' x_2' x_4' x_5' + x_1 x_2 x_4 x_5 + x_1' x_2' x_3 x_4' + x_1 x_2' x_3 x_5 + x_2' x_3' x_4 x_5' + x_1 x_2 x_3 x_4 x_5$$

$$n = x_2' x_3 x_4' + x_2' x_3' x_4' x_5' + x_1 x_3 x_4 x_5 + x_1 x_2' x_4 x_5' + x_1 x_3 x_4 x_5 + x_1' x_2' x_3' x_5' + x_1 x_2 x_3' x_4 x_5$$

FIGURE Q2(a)

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Technology: 0.8 μm twin-well CMOS
 Propagation delay signals < 1.2ns
 Transition times < 1.2 ns
 Circuit area < 1500 μm^2
 Dynamic power dissipation < 1mW

FIGURE Q3(a)

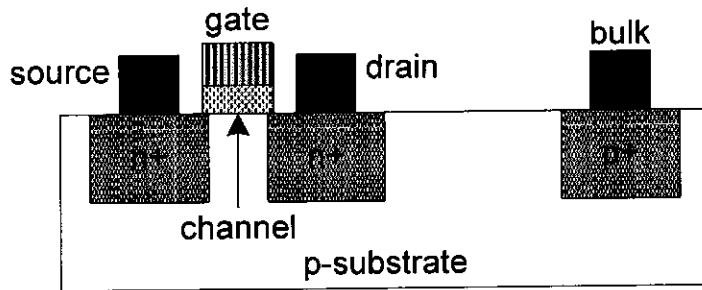
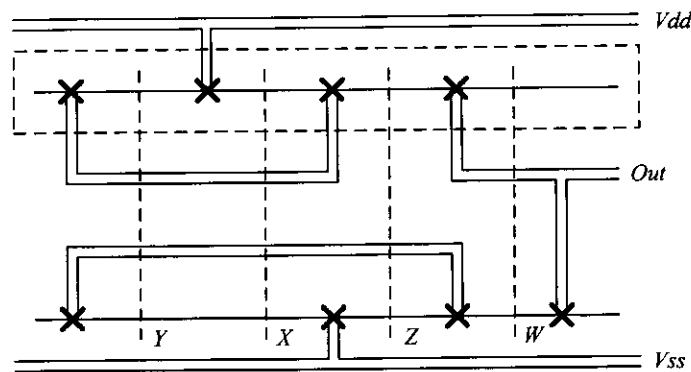


FIGURE Q5(a)



Legend:

	contact		nMOS
	metal		pMOS
	polysilicon		

FIGURE Q5(b)

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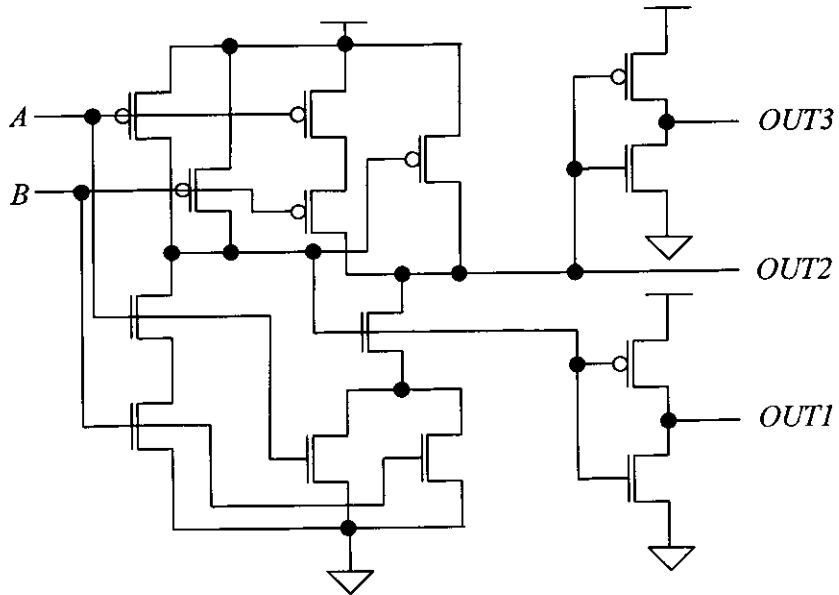


FIGURE Q6(a)

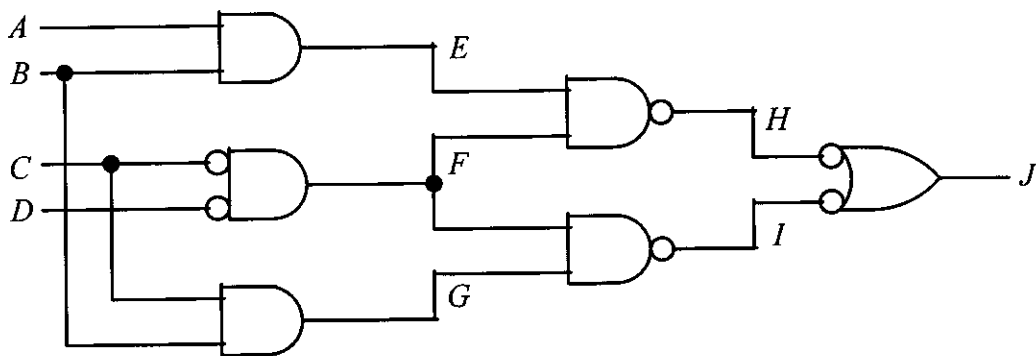


FIGURE Q9(b)