UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2010/11

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEX 21103/BEE 2233
PROGRAMME	:	2 BEE
EXAMINATION DATE	:	MAY 2011
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS PAPER CONSISTS OF FIVE (5) PAGES

Q1 (a) Give an example that is combination of both analog and digital system. Based on that example, explain how digital system less affected by noise.

(5 marks)

(b) Identify whether the following expression is True or False;

$$(A+B+\overline{C})\cdot(A+\overline{B}+C)\cdot(\overline{A}+B+C)\cdot(\overline{A}+\overline{B}+\overline{C}) = \overline{A \oplus B \oplus C}$$

(5 marks)

(c) Give the simplified Sum-of-Product (SOP) of the following expression;

$$F(A,B,C,D) = \Sigma\, m(4,8,9,12,13,14) + \Sigma\, d(0,1,2,5,10,15)$$

(5 marks)

Q2 (a) Show how an exclusive-NOR gate can be used to detect bit equality?

(3 marks)

(b) Write the Boolean expression for output X in **Figure Q2 (b)**. Determine the value of X for all possible input conditions and list the values in a truth table.

(6 marks)

(c) Interpret the following logic using only NAND gates;

$$V = W + \overline{\overline{\overline{X}} + Y + \overline{Z}}$$

(6 marks)

Q3 (a) Explain the main difference between Moore and Mealy state machines.

(3 marks)

(b) **Figure Q3 (b)** shows a 1-bit full adder. Demonstrate two (2) conditions of the propagated carry by using the diagram.

(4 marks)

(c) **Figure Q3 (c)** shows a 2-to-1 multiplexer. By using the block diagram, show how 3 units of 2-to-1 multiplexer can be cascaded to form a 4-to-1 multiplexer. Labels the resulting circuit completely.

(8 marks)

Q4 (a) Illustrate the basic operation of an encoder by the aid of a diagram.

(3 marks)

(b) **Figure Q4 (b)** shows a state diagram for a 2 bit up/down synchronous counter. The processor is equipped with input u which program the up-counting ($u=1$) and down counting ($u=0$). The 4 changing states are labeled as 2 bits that is 00,01,10 and 11 respectively. Produce the excitation table using Q_1Q_0 as our present state output and N_1N_0 as our next state output. Derive the simplest Boolean expression for all the J and K inputs.

(12 marks)

Q5 A bank has 3 independent locks and keys. Each key is owned by a different person that is the manager, accountant and security officer. In order to open the vault door, at least two people must insert their keys into the assigned lock simultaneously. Both manager and accountant can only open the vault with the presence of security officer. Three active LOW signal lines (A, B, C) will be activated upon the key insertion to locks 1, 2 and 3 respectively. The system will generate output HIGH (1) to unlock the vault.

(a) Derive the truth table for such a digital locking system

(8 marks)

(b) Design the logic circuit to realize the digital locking system

(7 marks)

(c) Implement the circuit obtained in Q5 (b) using two inputs NOR gate only

(5 marks)

Q6 (a) What makes latches and flip-flop differ? Discuss on latch and flip-flop advantages and disadvantages.

(6 marks)

(b) There are four (4) types of register. Differentiate the characteristics of these register using diagram.

(4 marks)

(c) The input frequency of a clock generator system is 144 kHz. The system is required to generate two frequencies 12 kHz and 2 kHz at its outputs. Propose an arrangement for frequency division by cascading 2 units of IC 74LS293 shown in **Figure Q6 (c)**.

(10 marks)

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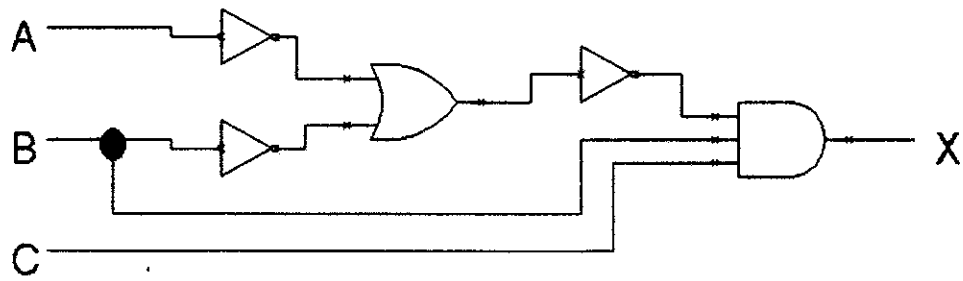

Figure Q2 (b)

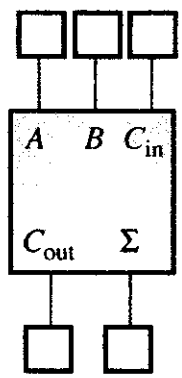

Figure Q3 (b)

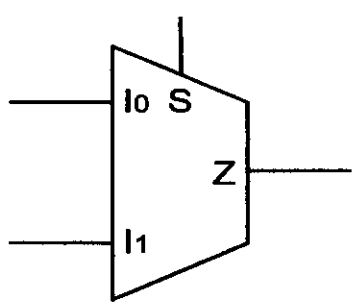

Figure Q3 (c)

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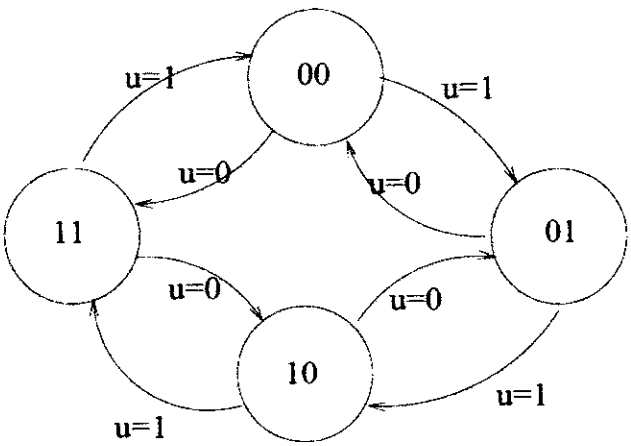

Figure Q4 (b)

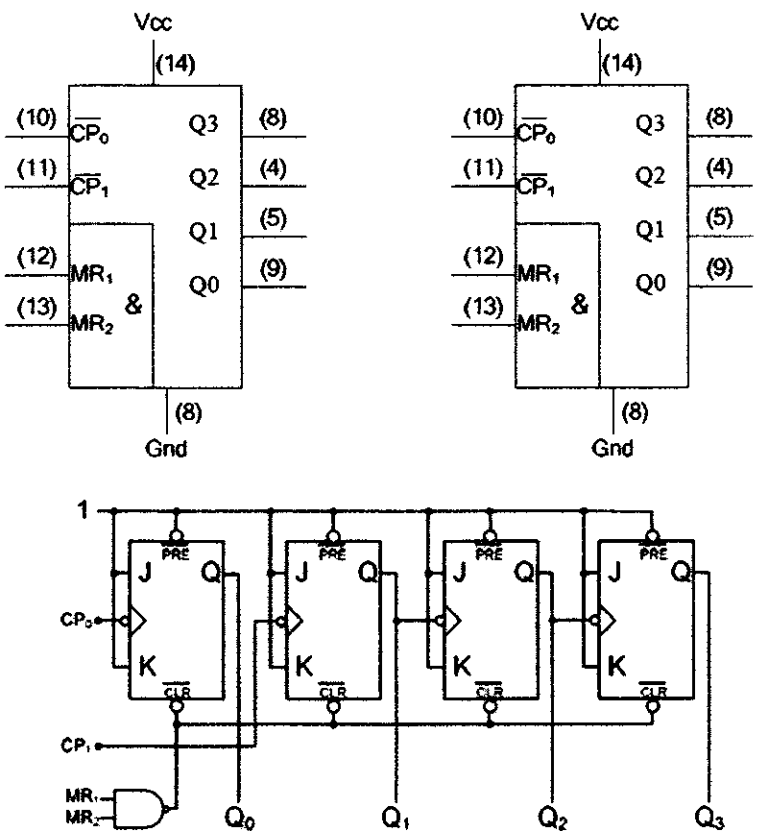

Figure Q6 (c)