UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2010/2011

COURSE	: ELECTRONIC DEVICES AND APPLICATION
COURSE CODE	: BEE 2273 / BEX 21003
PROGRAMME	: 2 BEE
EXAMINATION DATE	: NOVEMBER / DISEMBER 2010
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER **FIVE** (5) QUESTIONS ONLY.

THIS PAPER CONSISTS OF ELEVEN (11) PAGES

Q1 (a) Define the following parameters for op-amp:

(i) Differential voltage gain

(1 marks)

(ii) Common-mode voltage gain

(1 marks)

(b) Two experiments have been performed on the 741 IC and its results are as shown in Figure **Q1 (b)**. From the results, determine:

(i) common-mode voltage gain

(3 marks)

(ii) differential-mode voltage gain

(3 marks)

(iii) common mode rejection ratio (CMRR) in dB

(3 marks)

(c) A circuit is required to sum three signals v_1, v_2 and v_3 in the following manner:

$$V_{sum} = -(2\,v_1 + 5\,v_2 + 1.5\,v_3)$$

Design a circuit to perform this task.

(9 marks)

Q2 (a) Discuss the effects of negative feedback on amplifier characteristics.

(3 marks)

(b) Figure **Q2 (b)** is a voltage series feedback amplifier. Calculate the feedback factor, β and amplifier gain, A_f.

(4 marks)

(c) An audio amplifier with a negative feedback network as shown in Figure **Q2 (c)** has properties as follows:

Input impedance with feedback, $Z_{if} = 1\ k\Omega$
Output impedance with feedback, $Z_{of} = 100\ k\Omega$
Closed-loop gain, $A_f = 50$
Feedback factor = 0.01
Low cut off frequency with feedback, $f_{lf} = 2$ kHz
High cut off frequency with feedback, $f_{hf} = 200$ kHz
Input source voltage of amplifier = $40mV_{pp}$.

(i) Determine the gain without feedback, output impedance without feedback, output voltage and feedback voltage.

(6 marks)

(ii) In the same graph, sketch the frequency response for the amplifier, with and without feedback network.

(7 marks)

Q3 (a) Draw a general block diagram of sinusoidal oscillator and state the conditions that are required for a sustained state of oscillation.

(5 marks)

(b) Figure **Q3 (b)** is a Colpitts oscillator. If the circuit required to oscillate at 50 kHz, determine the value of L and R_F.

(5 marks)

(c) Figure **Q3 (c)** is a type of oscillator using two stages of op-amp. Given: $R_1 = R_3 = 10\ k\Omega$, $R_2 = 30\ k\Omega$, $C = 0.01\ \mu F$ and $V_{cc} = \pm 20\ V$.

(i) What is the difference between the oscillator in Figure **Q3 (b)** and Figure **Q3 (c)** in terms of the output waveform produced.

(1 marks)

(ii) Find the upper peak voltage (V_{UTP}) and lower peak voltage (V_{LTP}).

(3 marks)

(iii) Determine the frequency of oscillation.

(2 marks)

(iv) Sketch in parallel and label clearly the output voltage for both stages.

(3 marks)

(v) State the name of the oscillator circuit shown in Figure **Q3 (b)**.

(1 marks)

Q4 (a) The main part of internal circuit for a 555 timer is shown in Figure **Q4 (a)**. Based on the circuit shown, explain how an astable multivibrator can generate it output waveform.

(5 marks)

(b) Refer to the circuit in Figure **Q4 (b)**.

(i) State the mode of operation for 555 timers IC (A) and (B).

(1 marks)

(ii) Draw and label completely the waveforms of V_{C4}, V_{C2}, V_{01} and V_0. All waveforms must be drawn with their time axis in parallel.

(10 marks)

(iii) Determine the duty cycle for the 555 timer IC (A).

(2 marks)

(iv) Find the pulse width of the 555 timer IC (B).

(2 marks)

Q5 (a) Figure **Q5 (a)** shows a 12V power supply circuit. Identify four main parts of the power supply and briefly discuss their function.

(8 marks)

(b) A 10V voltage regulator experiences 12mV changes in output voltage when its input voltage changes to 5V. Beside that, it also experiences a 14mV changes in output voltage when load current increases from 0 to 100mA. Given that the full load voltage of the regulator is 9.986V.

(i) Determine the line regulation of the regulator in μV/V unit.

(2 marks)

(ii) Determine the load regulation of the regulator in μV/mA unit.

(2 marks)

(c) Figure **Q5 (c)** shows the circuit of step-down switching regulator. The voltage regulator is required to produce 4V DC voltage.

(i) Determine how long transistor Q1 must conduct at each cycle for switching frequency of 100 Hz. Lets $V_{IN} = 10V$.

(3 marks)

(ii) If the input voltage, V_{IN} increased to 12.5V, sketch the output waveform of PWM, V_{PWM}, to maintain the V_{OUT} at the regulated value.

(5 marks)

Q6 (a) Two op-amps are used in the circuit of Figure **Q6 (a)**. Both op-amps are powered by ± 10V. Based on that figure;

(i) state the name of this oscillator circuit.

(1 mark)

(ii) draw the output waveform obtained at V_{01}. Calculate the frequency of oscillation and find the value of R_F to obtain V_{01}.

(7 marks)

(iii) draw the output waveform V_{02} and clearly label it.

(7 marks)

(b) Determine the cutoff frequency for the filter shown in Figure **Q6 (b)**. State the filter type and the order, also draw the output frequency response. Indicate the roll-off of the frequency response.

(5 marks)

Q7 (a) Differentiate between Class A and Class B power amplifiers in terms of their operating cycle and efficiency in delivering power to the load.

(4 marks)

(b) The output waveform in Class B amplifier will have crossover distortion. Explain the crossover distortion. Using the aid of circuit diagram, describe a method that can be used to minimize or eliminate the distortion.

(8 marks)

(d) By using two dc power supplies of ±18V and a load resistor of 50Ω,

(i) design a basic Class B push pull amplifier.

(4 marks)

(ii) if its output signal has a peak value of 15 V, determine the efficiency and the dissipated power.

(4 marks)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

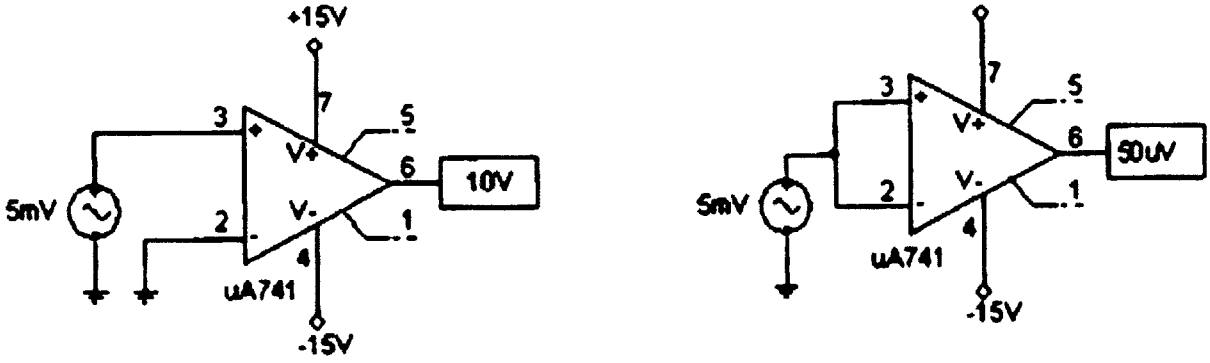

Figure Q1 (b)

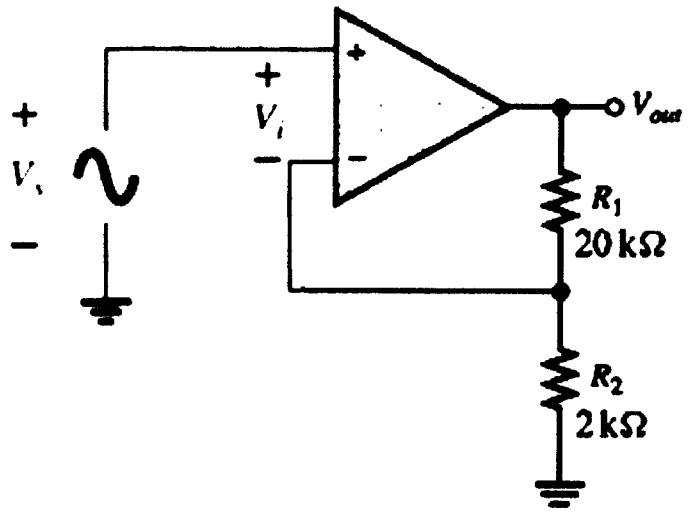

Figure Q2 (b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

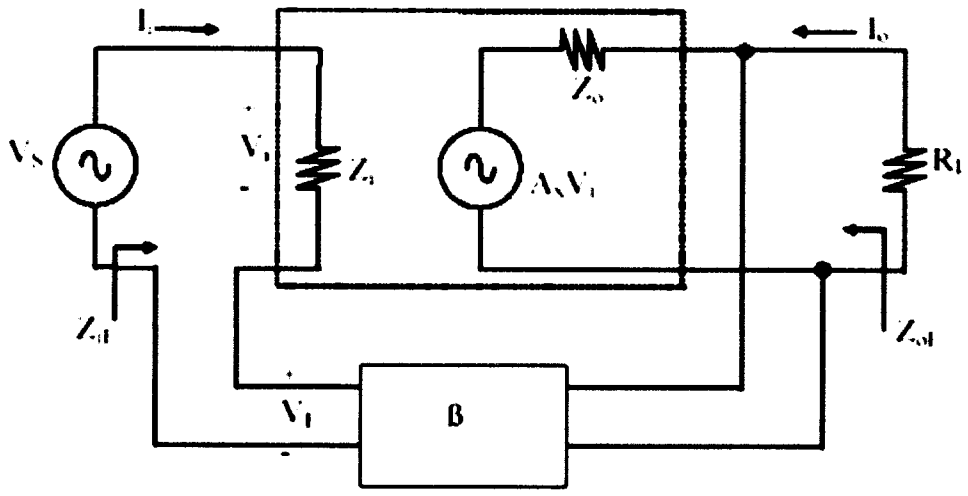

Figure Q2 (c)

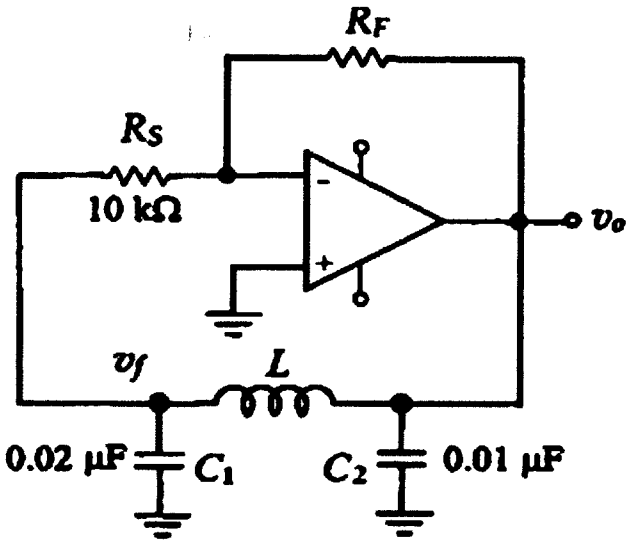

Figure Q3 (b)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

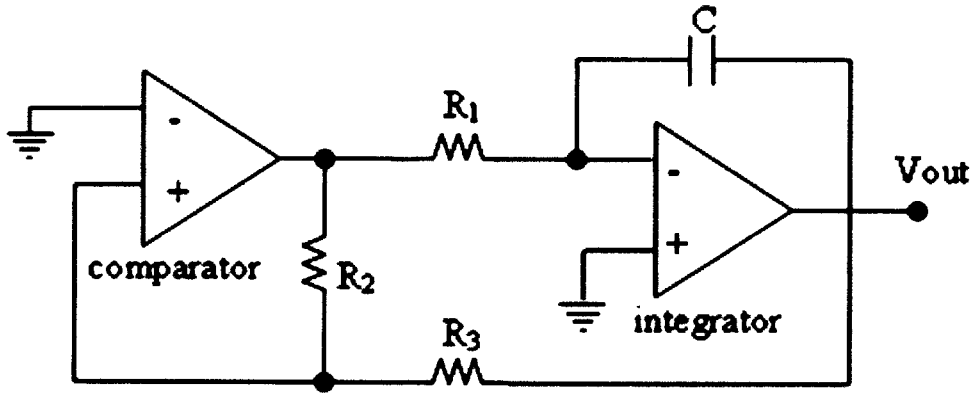

Figure Q3 (c)

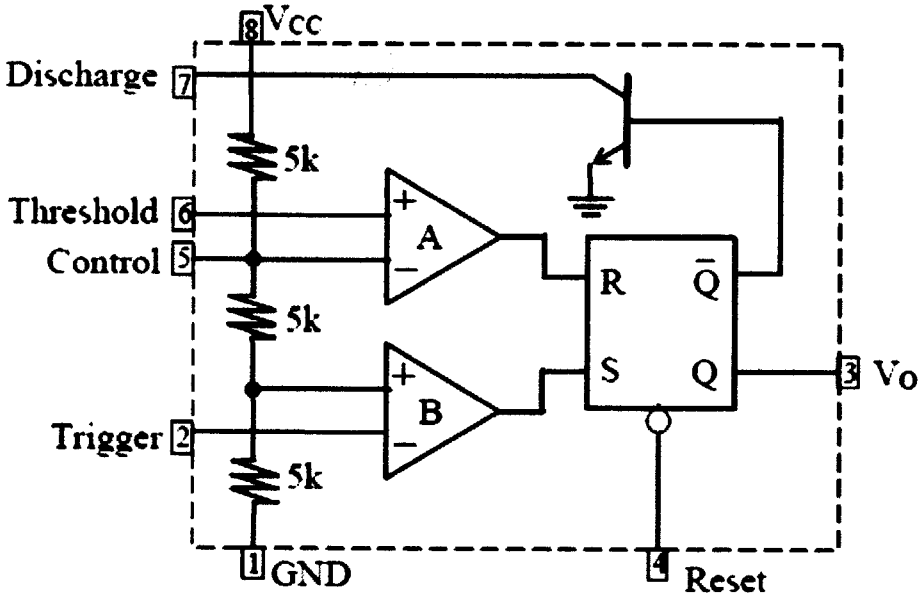

Figure Q4 (a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

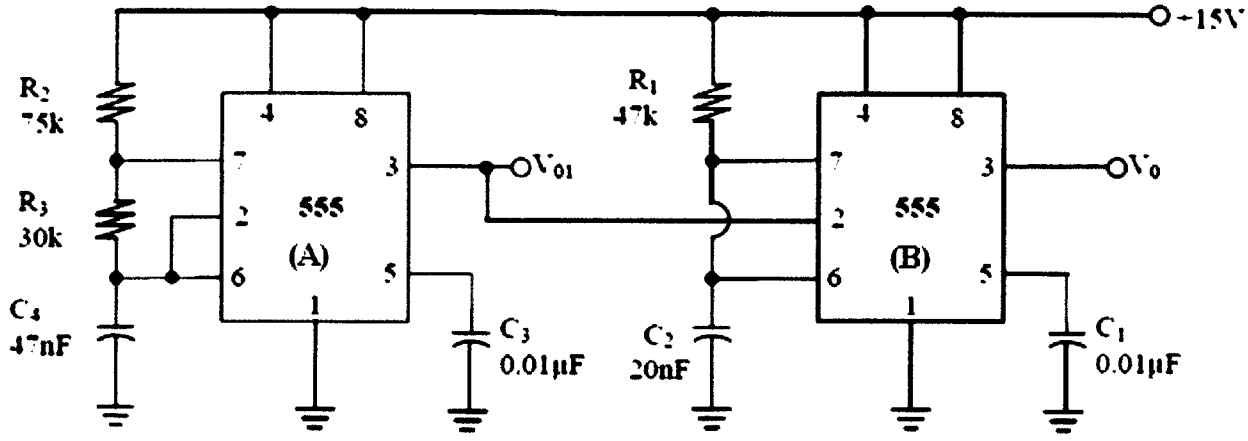

Figure Q4 (b)

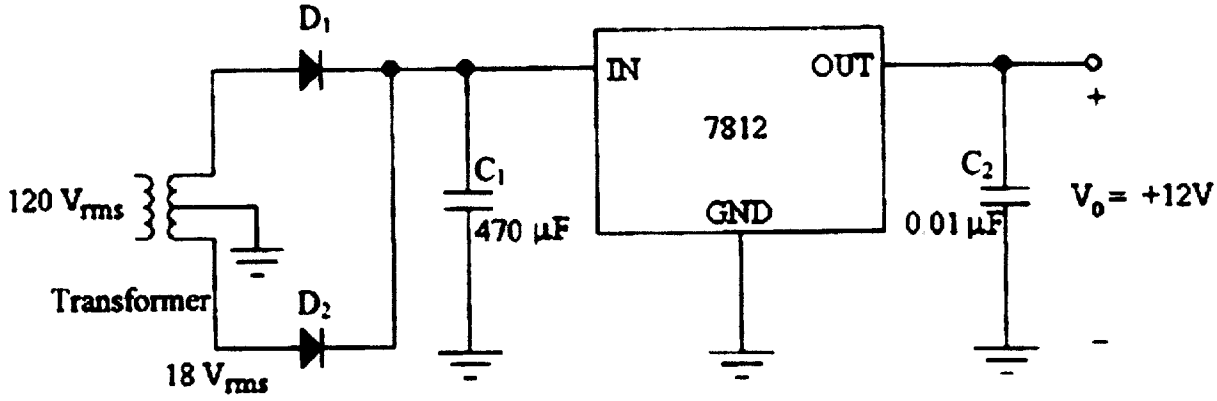

Figure Q5 (a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

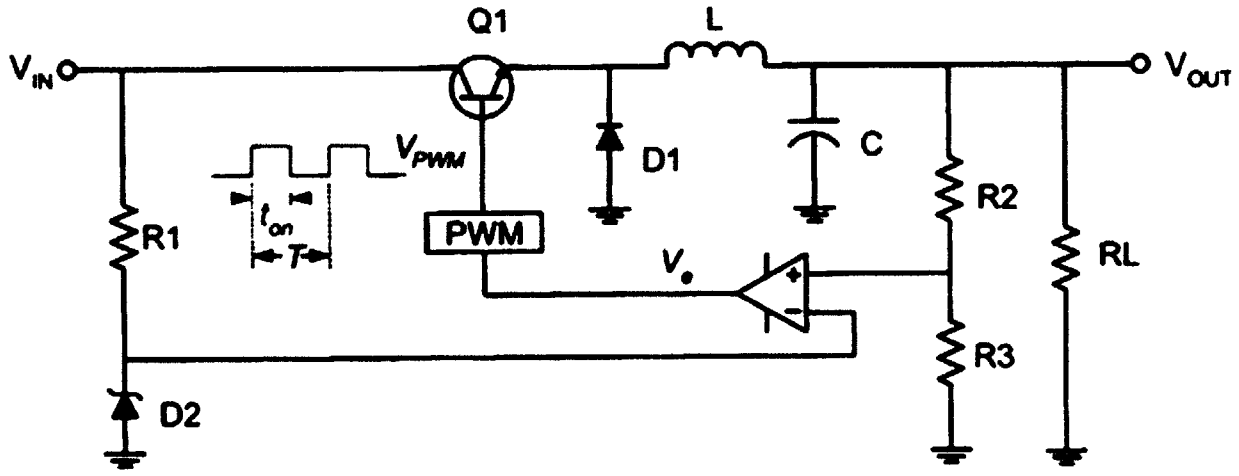

Figure Q5 (c)

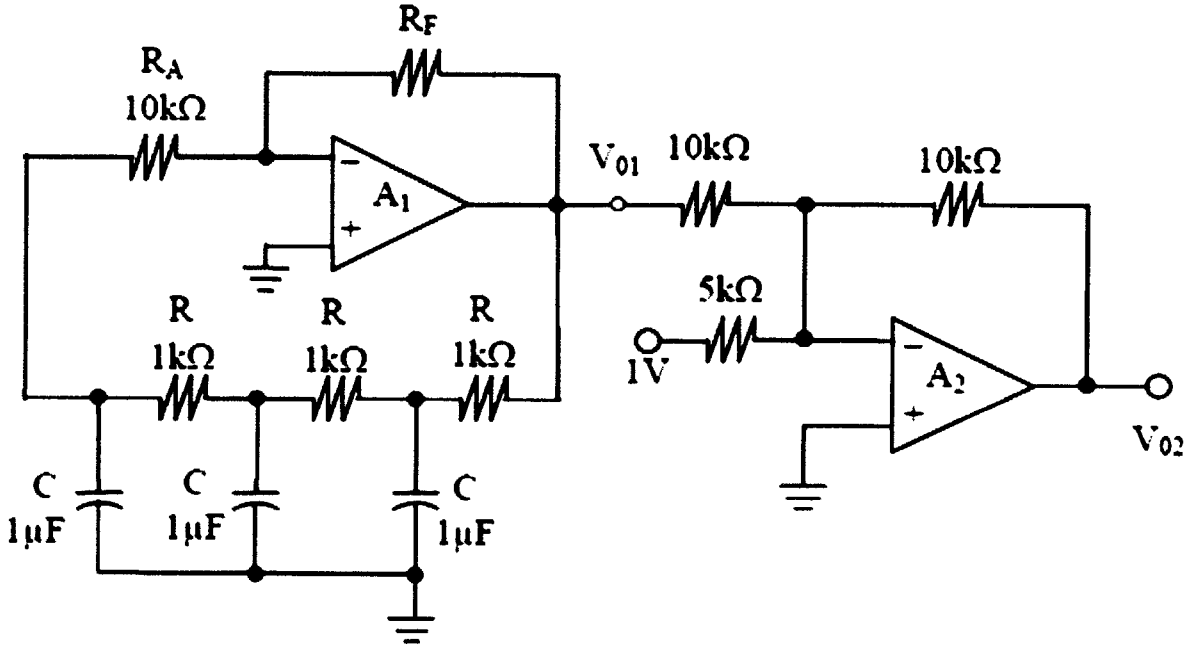

Figure Q6(a)

FINAL EXAMINATION

SEMESTER/SESSION: SEM I / 2010/2011 COURSE : 2 BEE
COURSE: ELECTRONIC DEVICES AND APPLICATION SUBJECT CODE: BEE2273/BEX 21003

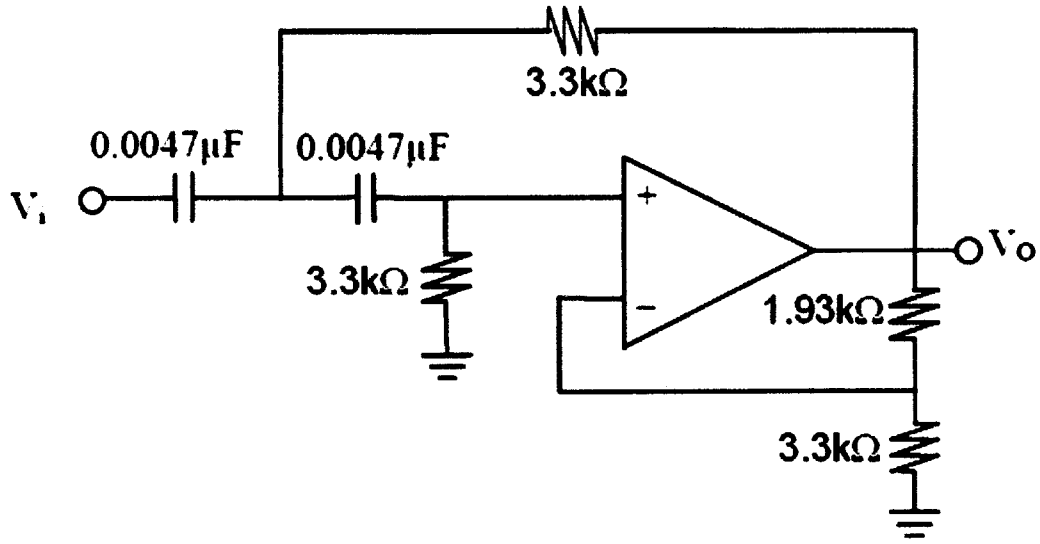

Figure Q6(b)