UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2010/2011

COURSE NAME	:	DIGITAL TECHNIQUE
COURSE CODE	:	BEF 12302
PROGRAMME	:	1 BEF
EXAMINATION DATE	:	NOVEMBER/DECEMBER 2010
DURATION	:	2½ HOURS
INSTRUCTION	:	ANSWER **4 (FOUR)** QUESTIONS ONLY

THIS EXAMINATION PAPER CONSISTS OF (8) PAGES

Q1

(a) Solve the following problem. Show all step.
(i) Convert binary 111000101001 to hexadecimal.
(ii) Convert octal 5328.10_8 to decimal.
(iii)Convert hexadecimal $E64B_{16}$ to octal

(9 marks)

(b) Briefly explain five (5) advantages of digital circuits compared to analog circuits

(10 marks)

(c) State two (2) advantages of using synchronous counter compared to asynchronous counter.

(4 marks)

(d) Using Boolean theorem, prove the following Boolean expression.

$$\overline{P \cdot \overline{Q} + \overline{P} \cdot Q} = \overline{P} \cdot \overline{Q} + P \cdot Q$$

(2 marks)

Q2

(a) Illustrate and prove how two half adder can be combined to form a full adder.

(7 marks)

(b) Using an appropriate example, explain the term of 'don't care' condition.

(4 marks)

(c) Prove that

$$(A + B + \overline{C}) \cdot (A + \overline{B} + C) \cdot (\overline{A} + B + C) \cdot (\overline{A} + B + C) \cdot (\overline{A} + \overline{B} + \overline{C}) = \overline{(A \oplus B \oplus C)}$$

(5 marks)

(d) Simplify the following equation

$$F = (b + d) \cdot (\overline{x} + \overline{y} + \overline{z})$$

(3 marks)

(e) Implement with a 2-input logic gates to produce the function in Q2(d) using only
(i) NOR gates
(ii) NAND gates

(6 marks)

Q3

(a) Figure Q3(a) shows a display of seven-segment indicator. Each segment of the indicator can be illuminated by applying logic 1 to the input for that segment. By simultaneously illuminating the appropriate segments, the device can be used to display from A to F. Construct a table whose seven outputs drive the seven-segment display. The circuit has three inputs, and the logic levels at this inputs represent the six (6) conditions (A, B, C, D, E, and F) in pure binary code.

(6 marks)

(b) Design an asynchronous counter using four (4) JK flip-flop for counting order as below. Assume that when turn on, the initial output (Q) for all flip-flop is LOW (0).

1001, 1000, 0111, 0110, 0101, 0100, 0011, 0010, 0001, 1001, 1000, ...

(5 marks)

(c) Figure Q3(c) shows a 4 stage frequency divider which form by a JK flip-flop. J and K input connected to HIGH (so it will always in toggle mode) are required for each stage.

(i) Draw the output signal of Q_A, Q_B, Q_C and Q_D of each stage by referring to input clock.

(ii) If the input clock is 100Hz, determine the frequency of Q_A, Q_B, Q_C and Q_D.

(8 marks)

(d) Determine and draw the state transition diagram for Moore machine in figure Q3(d).

(6 marks)

Q4

(a) Figure Q4(a) shows the state transition of a Mealy state machine. Input Y is the control input.

(i) Using notation QC (MSB), QB and QA for the states, build the state transition and state excitation table.

(ii) Using Karnaugh map, obtain the simplest Boolean expression for the all JK flip-flop (J and K input)

(iii)Draw the circuit.

(15 marks)

(b) A 4 bit shift register constructed from edge-triggered D-type flip flops is shown in figure Q4(b). If, on successive rising edges of the clock signal CLK, the input takes on the values 1, 0, 1, 0, 1, 1, 1, 0. Determine the contents of the shift register after each edge of the clock. You may assume that the register contains all zeroes initially.

(3 marks)

(c) The shift register in Q4(b) is require to detect '1011' bit pattern from the serial data fed into the input pin. Design and illustrate how the combinational logic circuit can be added to achieve this. This combinational logic circuit will produce an output HIGH (1) when the pattern is detected.

(7 marks)

Q5

(a) Figure Q5(a) shows a state transition diagram for an infinite state machine with control input, Y. Design the circuit using JK flip-flop.

(15 marks)

(b) Figure Q5(b) shows a 3 line-to-8 line (74LS138) decoder configured to implement a logic function. Obtain the simplest Boolean expression for Z.

(5 marks)

(c) Figure Q5(c) shows a 1 line-to-8 line Multiplexer (74LS151) configured to implement a logic function. Obtain the simplest Boolean expression for Y.

(5 marks)

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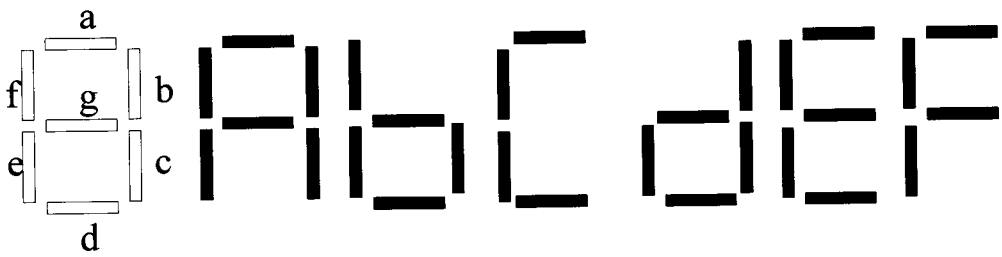

Figure Q3(a)

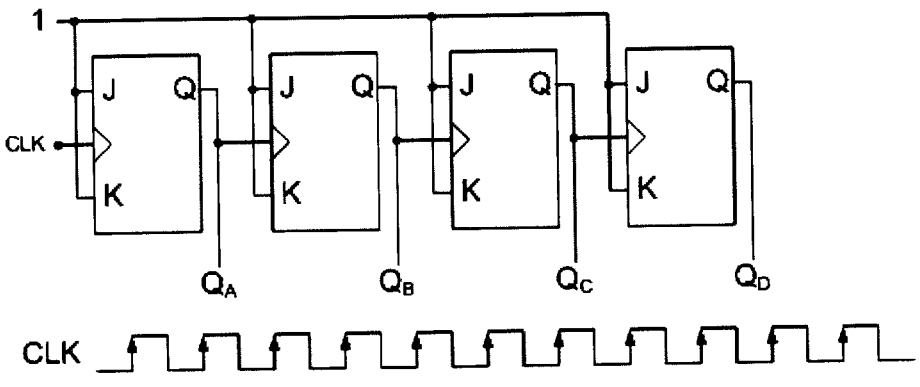

Figure Q3(c)

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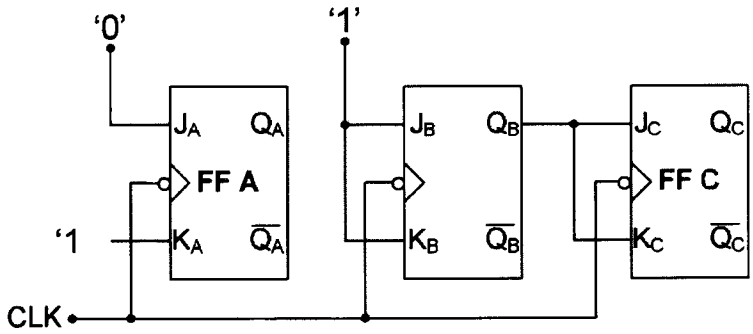

Figure Q3(d)

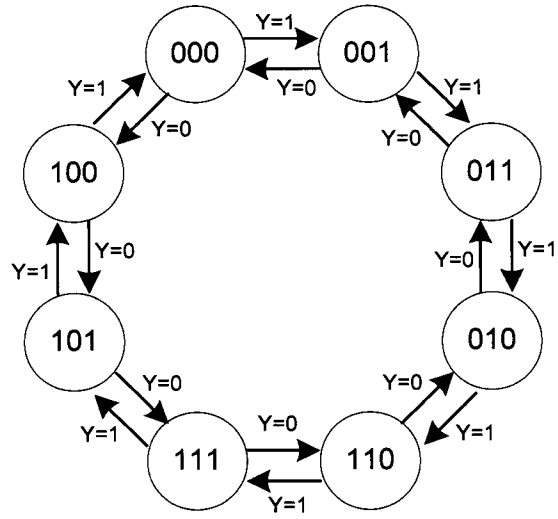

Figure Q4(a)

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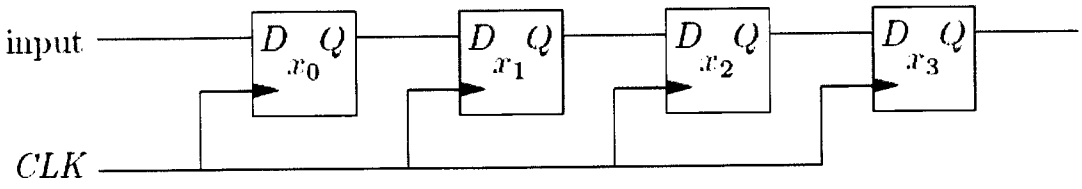

Figure Q4(b)

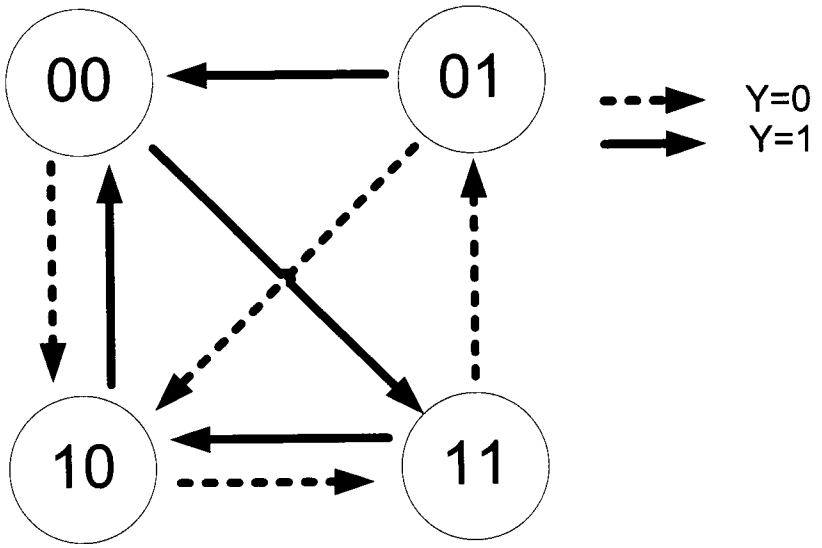

Figure Q5(a)

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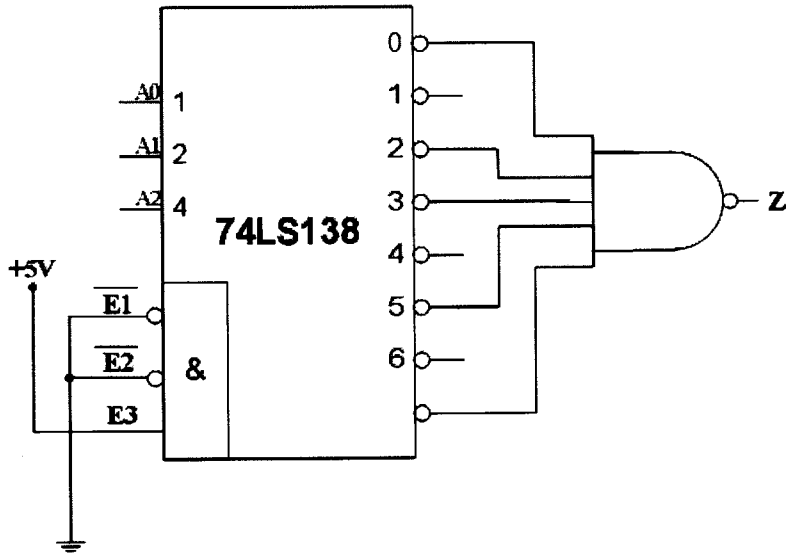

Figure Q5(b)

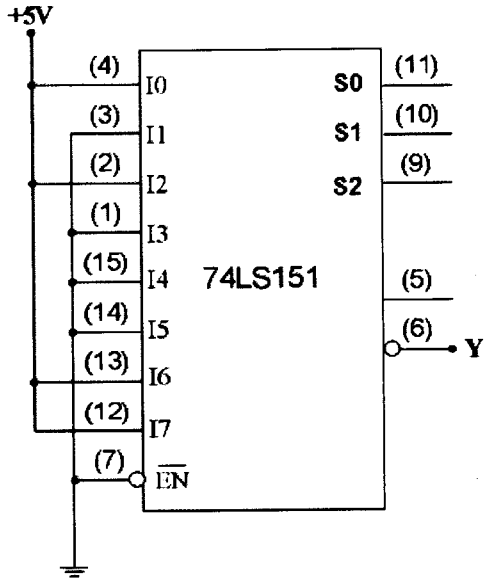

Figure Q5(c)