UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2010/2011

COURSE	: DIGITAL SYSTEM DESIGN
COURSE CODE	: BEE 3133
PROGRAMME	: 3BEE
EXAMINATION DATE	: NOVEMBER / DECEMBER 2010
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER ALL QUESTIONS IN PART A AND THREE (3) QUESTIONS ONLY IN PART B.

THIS PAPER CONSISTS OF NINE (9) PAGES.

PART A

Q1 Very-Large-Scale Integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip.

(a) State three (3) critical VLSI design considerations.

(3 marks)

(b) Give three (3) reasons why the CMOS technology leading in IC market.

(3 marks)

(c) Give two (2) differences between top down and bottom up approach.

(4 marks)

(d) Propose two (2) solutions for these common design problems:

(i) The growing number of transistor in IC design.
(ii) Cross talk in circuit design.
(iii) High interconnect delay.

(6 marks)

(e) The following are VLSI design styles; Full Custom, Application -Specific Integrated Circuit (ASIC), Programmable Logic (PLD, FPGA) and System-on-a chip (SoC). Briefly explain any two (2) of them.

(4 marks)

Q2 Suppose that the test set $w_1 w_2 w_3 w_4 = 0100, 1010, 0011, 1111$ *and* 0110 are chosen randomly to test the circuit in Figure Q2. Find the percentage of single faults can be detected using these tests.

(20 marks)

PART B

Q3 (a) Determine all the subcircuits defined in the VHDL code in Figure Q3(a).
(2 marks)

(b) Explain the purpose of signal in VHDL code.
(2 marks)

(c) Draw the schematic diagram for the circuit represented by the VHDL description in Figure Q3(a).
(16 marks)

Q4 (a) Given a function, $G = A\overline{C}E + A\overline{C}F + A\overline{D}E + A\overline{D}F + BCD\overline{E}\overline{F}$. Assume that the input variables are available in both uncomplemented and complemented forms.

(i) Determine the Boolean expression by using factoring technique.
(3 marks)

(ii) Determine the Boolean expression by using functional decomposition technique.
(3 marks)

(iii) Sketch the circuit for the Boolean expression in Q4(a)(ii) and calculate the cost.
(5 marks)

(b) Map the following function in a Karnaugh map.

$F(a,b,c,d,e) = \Sigma m(0, 3, 4, 5, 6, 7, 8, 12, 13, 14, 16, 21, 23, 24, 29, 31)$

Based on the K-map,

(i) Find the minimum Sum-of-Product.
(5 marks)

(ii) Find the Product-of-Sum equation based on question Q4(b)(i).
(4 marks)

Q5 (a) The architecture log VHDL contains the code that is synthesized into hardware. It describes the behavior of the model.

(i) Architecture contains the synthesizable code, and must be written correctly. There are three (3) major classifications for architecture declaration. List them.

(3 marks)

(ii) List two (2) assignment statements for Behavioral Modeling.

(2 marks)

(iii) Concurrent statement is used to assign a value to a signal in an architecture body. VHDL provides four (4) different types of concurrent statements. List these statements.

(2 marks)

(b) A multiplexer is a logic component that has several inputs but only a single output. The purpose of the multiplexer circuit is to multiplex the *n* data inputs onto the single data output under control of the select inputs. The functionality of 4-to-1 multiplexer (referred as 4:1 mux) can be described in the truth table in Figure Q5(b)(a). The bit represented by S_1 and S_0 selects one of the data inputs as the output of the multiplexer. Construct the VHDL code in architecture statement for the truth table using:

(i) Selected assignment.

(4 marks)

(ii) Conditional assignment.

(4 marks)

(iii) IF statement.

(5 marks)

Q6 (a) CMOS stand for Complementary Metal Oxide Semiconductor.

(i) What is the advantage of CMOS structure?

(2 marks)

(ii) Justify your reason in proposing the construction with visual aid.

(5 marks)

(b) Figure Q6(b) shows half of a CMOS circuit.

(i) Construct truth table for the circuit.

(6 marks)

(ii) Derive the simplest sum-of-products expression for the truth table in part Q6(b)(i).

(3 marks)

(iii) Derive the other half that contains the PMOS transistors.

(4 marks)

Q7 Refer to the waveform in Figure Q7.

(a) Derive the simplest Boolean expression by using K-map.

(3 marks)

(b) Construct minimum transistor level circuit using CMOS technology.

(6 marks)

(c) Determine either the circuit in Q7(b) is AOI or OAI.

(2 marks)

(d) Draw the Euler path for the circuit.

(4 marks)

(e) Sketch the stick diagram for the circuit.

(5 marks)

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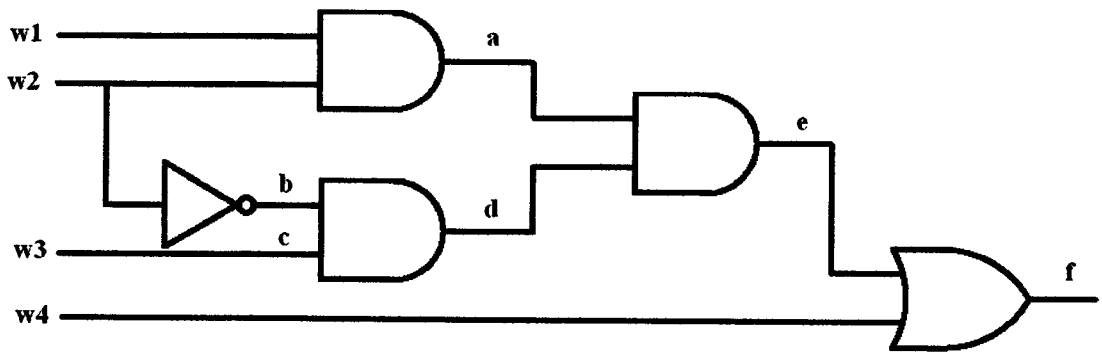

Figure Q2

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```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY litar IS
PORT(w : IN STD_LOGIC_VECTOR(0 TO 15);
     s : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
     a,b,c,d,e : IN STD_LOGIC;
     f : OUT STD_LOGIC);
END litar;

ARCHITECTURE structure OF litar IS
SIGNAL m : STD_LOGIC_VECTOR(0 TO 3);
SIGNAL y : STD_LOGIC_VECTOR(0 TO 3);

COMPONENT mux4to1
PORT(w0,w1,w2,w3 : IN STD_LOGIC;
     s           : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
     f           : OUT STD_LOGIC);
END COMPONENT;

COMPONENT my_chip
PORT(x,y : IN STD_LOGIC;
     z   : OUT STD_LOGIC);
END COMPONENT;

BEGIN
Chip1: my_chip PORT MAP (y(0),y(1),m(0));
Chip2: my_chip PORT MAP (a,b,m(1));
Chip3: my_chip PORT MAP (y(2),y(3),m(2));
m(3)<= (not c and not d) or e;
Mux1: mux4to1 PORT MAP (w(0),w(1),w(2),w(3),s(1 DOWNTO 0),y(0));
Mux2: mux4to1 PORT MAP (w(4),w(5),w(6),w(7),s(1 DOWNTO 0),y(1));
Mux3: mux4to1 PORT MAP (w(8),w(9),w(10),w(11),s(1 DOWNTO 0),y(2));
Mux4: mux4to1 PORT MAP (w(12),w(13),w(14),w(15),s(1 DOWNTO
0),y(3));
Mux5: mux4to1 PORT MAP (m(0),m(1),m(2),m(3),s(3 DOWNTO 2),f);
END structure;
```

Figure Q3(a)

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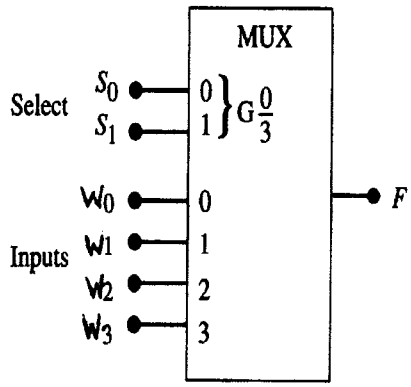
S1	*S0*	*f*
0	0	*w0*
0	1	*w1*
1	0	*w2*
1	1	*w3*

(a)



(b)

Figure Q5(b)

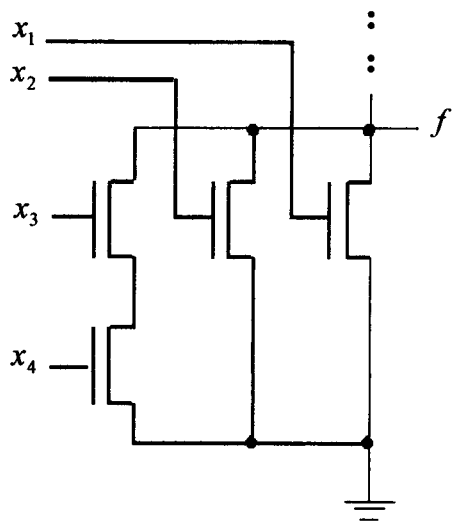


Figure Q6(b)

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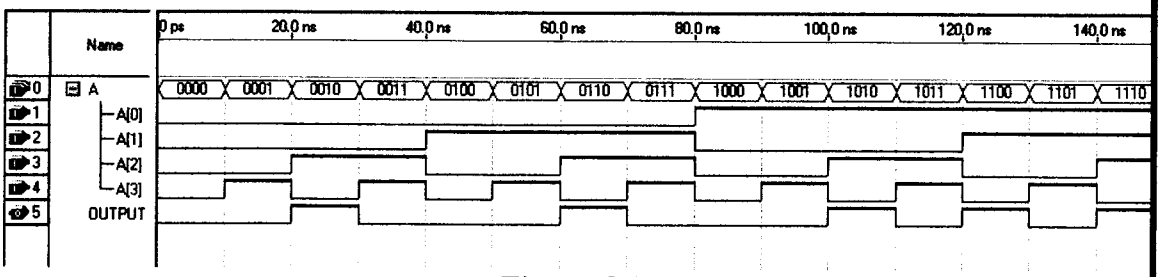

Figure Q7