



UNIVERSITI TUN HUSSEIN ONN MALAYSIA

PEPERIKSAAN AKHIR SEMESTER II SESI 2009/2010

NAMA KURSUS	:	MIKROPENGAWAL
KOD KURSUS	:	DEK 3133
PROGRAM	:	3 DET,DEE
TARIKH PEPERIKSAAN	:	APRIL/MEI 2010
JANGKAMASA	:	3 JAM
ARAHAN	:	JAWAB SEMUA SOALAN DI BAHAGIAN A DAN JAWAB DUA (2) SOALAN DI BAHAGIAN B

KERTAS SOALANINI MENGANDUNGI DUA PULUH (20) MUKA SURAT

SOALAN DALAM BAHASA MALAYSIA

BAHAGIAN A

- SI** (a) Nyatakan **definisi** bagi Mikropengawal dan berikan empat (**4**) **perkara** yang perlu diberi perhatian untuk memilih Mikropengawal yang sesuai. (5 markah)
- (b) Rajah **S1(b)** adalah struktur ingatan sebuah Mikropengawal. Terdapat 8 talian data dan 13 talian alamat yang dihubungkan antara CPU dan ingatan. Dengan mengambil kira 1Kb adalah bersamaan 1024bait.
- (i) Kirakan saiz ruangan ingatan tersebut.
(ii) Apakah jenis talian bas yang akan menentukan saiz ingatan sebuah Mikropengawal. (4 markah)
- (c) Lakarkan sebuah litar Mikropengawal PIC16F877A yang mempunyai masukan papan kekunci 4x3. (5 markah)
- (d) Sekiranya anda menggunakan pemasa *TMR0* bersama pengayun berkelajuan 10MHz dan *Prescaler* 1:64, **kirakan masa** yang diperlukan untuk *TMR0* menghasilkan satu (1) limpahan dengan kiraan *TMR0* bermula dari 200. (5 markah)
- (e) PIC16F877A menggunakan bekalan jam berfrekuensi 22MHz.
- (i) **Tunjukkan pengiraan** untuk mengetahui tempoh masa yang diambil oleh Mikropengawal menyelesaikan satu (1) suruhan.
(ii) **Berapakah** suruhan yang mampu dilaksanakan oleh Mikropengawal dalam tempoh $10.0\mu s$ dan $200.0\mu s$? (6 markah)

- S2 (a) PIC16F877A mempunyai resolusi 10-Bit ($0b1111111111=1023$) bagi penukaran analog kepada digital. Voltan rujukan adalah 4V, tentukan nilai **Saiz Langkah** dan **Keluaran Digital** bagi *ADC* tersebut sekiranya voltan masukan analog adalah 2V. Berikan jawapan dalam nombor binari mengikut turutan *bit*. (8 markah)
- (b) Sekiranya saiz ingatan *'EEPROM'* sesebuah Mikropengawal adalah 256byte. **Tentukan arahan MikroC** yang sesuai untuk memenuhkan keseluruhan ruangan ingatan tersebut dengan nilai $0b01010101$. (6 markah)
- (c) Rajah S2(c) menunjukkan dua Mikropengawal yang berhubung antara satu sama lain dengan menggunakan modul perkakasan *USART*. **Tentukan arahan MikroC** yang membolehkan Mikropengawal B **membunyikan buzzer BUZ1** sekiranya butang B1 ditekan pada Mikropengawal A. Kelajuan penghantaran yang digunakan adalah 9600 *bit/s*. Bina kod aturcara bagi kedua-dua Mikropengawal. (7 markah)
- (d) Merujuk pada Rajah S2(d), sebuah MOTOR DC disambung kepada modul *PWM* pada frekuensi 20Khz. **Tentukan arahan MikroC** supaya putaran MOTOR tersebut adalah 80 peratus daripada kelajuan asalnya. (4 markah)

BAHAGIAN B

S3 Rajah S3 menunjukkan sebuah sistem kawalan untuk mengekalkan suhu sebuah bilik pada tahap 40°C hingga 50°C . Sistem ini menggunakan penderia suhu yang mengukur suhu di antara 0°C - 100°C . Keluaran litar penderia suhu adalah voltan analog ($0\text{V}-5\text{V}$) yang merupakan masukan kepada litar Mikropengawal. Terdapat dua komponen keluaran LED dan speaker yang berfungsi sebagai petunjuk kepada nilai suhu semasa dan sebuah kipas yang berfungsi untuk menurunkan suhu bilik sekiranya suhu tertentu dicapai. LED, kipas dan speaker akan berfungsi berdasarkan Jadual S3. Voltan rujukan Mikropengawal adalah 5V .

(a) Tentukan :

- (i) Saiz Langkah.
- (ii) Nilai ADC apabila nilai V_m pada AN0 adalah 1.3V .
- (iii) Nilai suhu dalam *Celsius* sekiranya $V_m = 1.3\text{V}$

(5 markah)

(b) Sekiranya PIC menggunakan Voltan rujukan $+5\text{V}$, tuliskan aturcara *MikroC* yang menghasilkan proses penukaran analog kepada digital dan seterusnya dapat mengawal suhu bilik.

(20 markah)

S4 Litar dalam Rajah S4 beroperasi dengan memaparkan turutan nyalaan *Running Light* samada turutan atas ke bawah atau bawah ke atas dengan sela masa setiap LED selama satu saat. Bagi LEDTMR0 pula, ia akan sentiasa berkelip setiap dua (2) saat. Pemasa lengahan PIC adalah daripada pemasa TMR0 dengan skala 1:64 dan nilai awalan TMR0 adalah 0. Sekiranya PIC dibekalkan pengayun (*Fosc*) dengan frekuensi 65536Hz .

(a) Tentukan:

- (i) Tempoh masa bagi limpahan TMR0 bermula dari 0 hingga 255.
- (ii) Bilangan limpahan TMR0 yang diperlukan untuk mendapatkan tempoh lengahan selama satu (1) saat.

(5 markah)

(b) Dengan menggunakan pemasa TMR0 binakan kod pengaturcaraan *MikroC* di mana LEDTMR0 akan berkelip setiap dua (2) saat manakala setiap LED *Running Light* akan berkelip setiap satu (1) saat dengan menggunakan arahan *Delay_ms()*.

(20 markah)

S5 Litar dalam Rajah S5 beroperasi dengan memaparkan arah putaran motor pada paparan LCD dan pada nyalaan LED apabila butang arah putaran ditekan.

- (a) (i) Terangkan fungsi pemacu ULN2003A.
(ii) Tentukan bagaimanakah kelajuan sesebuah *STEPPER MOTOR* boleh dikawal? (5 markah)
- (b) Binakan **kod pengaturcaraan MikroC** di mana *stepper motor* akan berpusing mengikut arah butang yang ditekan dan seterusnya LED dan *LCD* akan memaparkan arah putaran yang dipilih. (20 markah)

SOALAN DALAM BAHASA INGGERIS**PART A**

- Q1** (a) Give definition of Microcontroller and give four (4) important aspects required attention to choose suitable Microcontroller. (5 marks)
- (b) Figure **Q1(b)** shows the memory structure of microcontroller. There are 8 data buses and 13 address buses connected between CPU and memory. Considering 1Kb is equal to 1024bytes:
- (i) Calculate the size of the memory for thus microcontroller.
 - (ii) Identify what type of buses will determine the memory size of the microcontroller?
- (4 marks)
- (c) Draw a circuit of Microcontroller PIC16F877A with keypad 4x3 as input. (5 marks)
- (d) If you use TMR0 timer with 10MHz Oscillator and Prescaler 1:64, **calculate the time required** for TMR0 to produce one (1) Overflow when TMR0 started from 200. (5 marks)
- (e) A PIC16F877A uses a clock frequency of 22MHz.
- (i) **Show the calculation** to know a time period taken by Microcontroller to complete one (1) instruction
 - (ii) **How many Instructions** can be executed by microcontroller within $10.0\mu s$ and $200.0\mu s$?
- (6 marks)

Q2 (a) A PIC16F877A has 10-Bit resolutions ($0b11111111=1023$) for analog to digital conversion (ADC). By using the voltage reference of 4V, determine the **Step Size** and **Digital Output** of ADC when the analog input is 2V. Express your answer in binary format by following the bit order.

(8 marks)

(b) If the Microcontroller's EEPROM size is 256byte, identify the suitable **MikroC instruction** to load all the memory space with value of $0b01010101$.

(6 marks)

(c) Figure S2 (c) are two Microcontroller interconnect between each other using the USART module hardware. Give the instructions of *MikroC* that allows the Microcontroller B to produce sound on buzzer **BUZ1** when button **B1** at Microcontroller A is pressed. Speed transmission used is 9600 bits/s. Construct your code for both microcontroller.

(7 marks)

(d) By Referring to Figure S2(d), a DC MOTOR is connected to the PWM module at frequency 20Khz. Determine the instructions of *MikroC* to rotate the MOTOR about 80 percent of its original speed.

(4 marks)

PART B

Q3 Figure Q3 shows a control system to maintain room temperature between 40°C to 50°C. The system is used a temperature sensor to measure the temperature between 0°C to 100°C. The output of temperature sensor is analog voltage (0V-5V) which is the input to the PIC circuit. There are two output (LED & Speaker) which work as indicator for the current temperatures level and a fan which operate to cool down the room temperature when a certain temperature is achieved. LED, speaker and fan will functioned based on Table S3. Voltage reference used by PIC is 5V.

(a) Evaluate:

- (i) Step size value.
- (ii) ADC result when V_{in} to AN0 is 1.3V.
- (iii) Temperature Value in degree *Celsius* when $V_{in} = 1.3V$.

(5 marks)

(b) If the PIC uses voltage reference of +5V, produce a **C program** to show the conversion process from analog to digital and then control the room temperature.

(20 marks)

Q4 Circuit in Figure Q4 operates by showing the LED lit in running light sequence with interval one(1) second for each LEDs whether from top to down or down to top . The LEDTMR0, it's always blinking every two (2) second. Delay Timer PIC is from Hardware Timer (TMR0) with prescaler 1:64 and preload value TMR0 is set to 0. If the PIC is provided with Oscillator frequency (Fosc) 65536 Hz,

(a) Determine:

- (i) The time taken for TMR0 to overflow starting from 0 to 255.
- (ii) Number of TMR0 overflows required to get 1 second delay.

(5 marks)

(b) By using the TMR0 Timer write a **MikroC program** to ensure that the LEDTMR0 will blinking every two (2) second, while the running light LEDs will running with interval one (1) second by using *Delay_ms()* instruction.

(20 marks)

- Q5** Circuit in Figure Q5 operates by showing the direction of stepper motor rotation into LCD display and also on LED when one of the direction buttons is pressed.

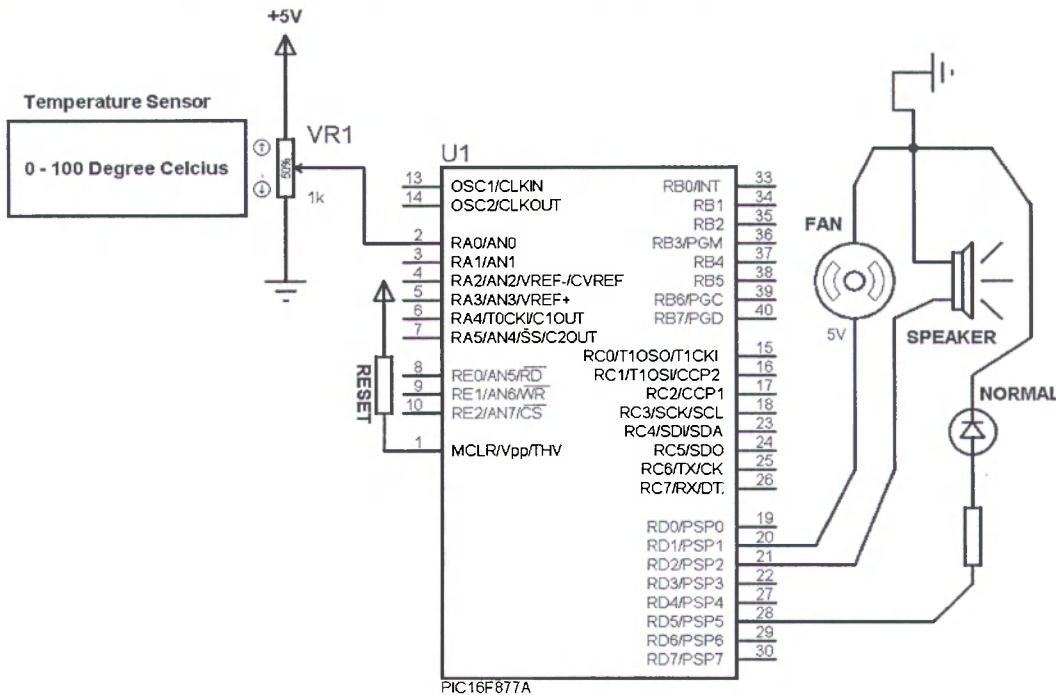
(a) (i) Explain the function of ULN2003A driver.
(ii) Evaluate how the speed of stepper motor can be controlled?. (5 marks)

(b) Develop a MikroC program to rotate the stepper motor with direction of button pressed and show the direction of rotation on LED and LCD. (20 marks)

PEPERIKSAAN AKHIR

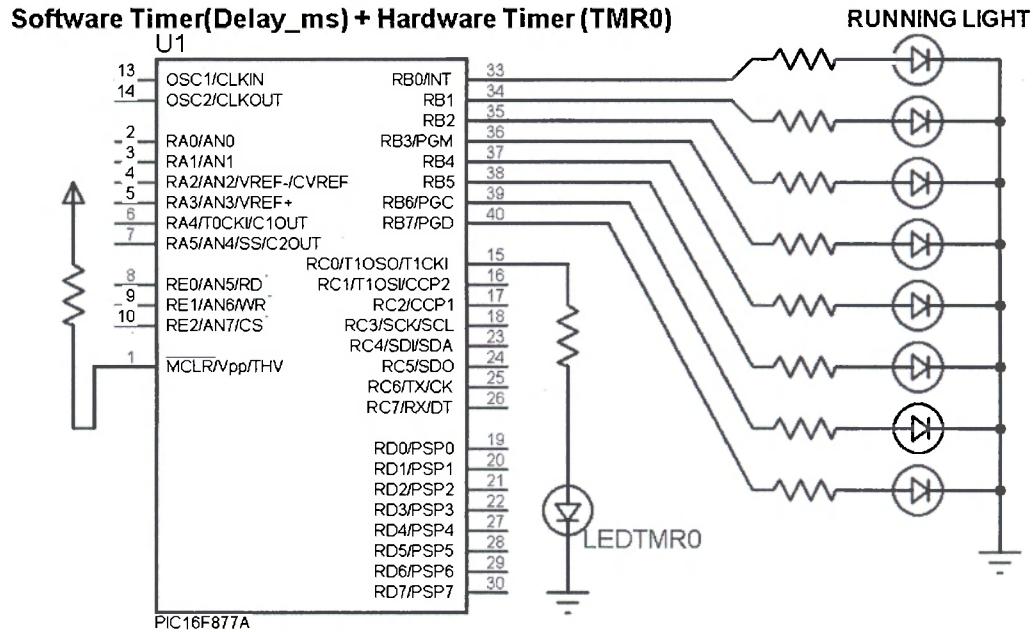
SEMESTER/SESI : SEMESTER II/2009/10
 MATAPELAJARAN : MIKROPENGAWAL

KURSUS : 3 DET,DEE
 KOD MP : DEK 3133

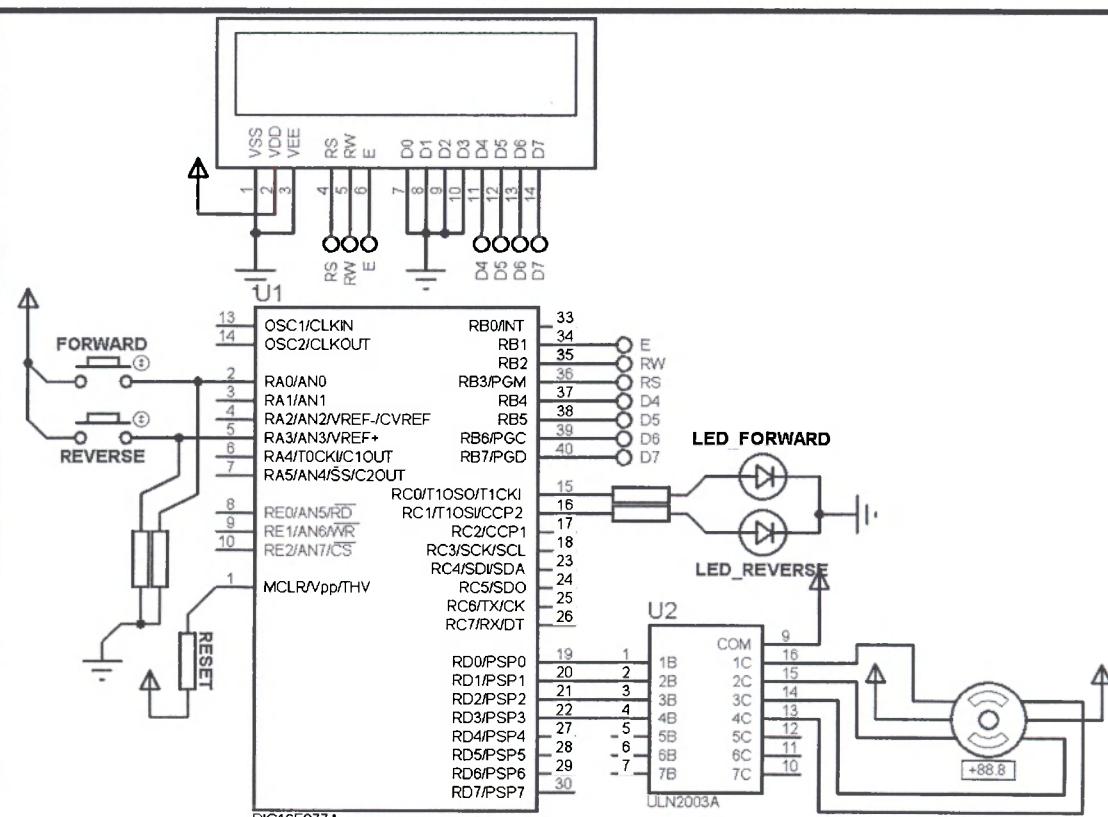
**Rajah S3 / Figure Q3**

Temperatures	LED and Fan Status
Above 50°C	Fan = Rotate, Speaker = ON, LED Normal = OFF
Below 45°C	Fan = Stop, Speaker = MUTE
Below 40°C	LED Normal = ON

Jadual S3 / Table Q3

PEPERIKSAAN AKHIRSEMESTER/SESI
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: MIKROPENGAWALKURSUS : 3 DET,DEE
KOD MP : DEK 3133**Rajah S4 / Figure Q4**

PEPERIKSAAN AKHIR

SEMESTER/SESI
MATAPELAJARAN: SEMESTER II/2009/10
: MIKROPENGAWALKURSUS : 3 DET,DEE
KOD MP : DEK 3133

Rajah S5 / Figure Q5

Forward	Step #	1B	2B	3B	4B	Reverse
		1	0	0	1	
	1	1	0	0	0	
	2	1	1	0	0	
	3	1	0	1	0	
	4	0	1	0	0	
	5	0	1	1	0	
	6	0	0	1	0	
	7	0	0	1	1	
	8	0	0	0	1	

Jadual S5/ Table Q5

PEPERIKSAAN AKHIR

SEMESTER/SESI
MATAPELAJARAN

: SEMESTER II/2009/10
: MIKRO PENGAWAL

KURSUS : 3 DET,DEE
KOD MP : DEK 3133

RUJUKAN I

FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP

File Address	File Address	File Address	File Address
Indirect addr. ⁽¹⁾	00h	Indirect addr. ⁽¹⁾	80h
TMR0	01h	OPTION REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
PORTA	05h	TRISA	85h
PORTB	06h	TRISB	86h
PORTC	07h	TRISC	87h
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h
PORTE ⁽¹⁾	09h	TRISE ⁽¹⁾	89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
PIR2	0Dh	PIE2	8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh		8Fh
T1CON	10h		90h
TMR2	11h	SSPCON2	91h
T2CON	12h	PR2	92h
SSPBUF	13h	SSPADD	93h
SSPCON	14h	SSPSTAT	94h
CCPR1L	15h		95h
CCPR1H	16h		96h
CCP1CON	17h		97h
RCSTA	18h	TXSTA	98h
TXREG	19h	SPBRG	99h
RCREG	1Ah		9Ah
CCPR2L	1Bh		9Bh
CCPR2H	1Ch	CMCN	9Ch
CCP2CON	1Dh	CVRCON	9Dh
ADRESH	1Eh	ADRESL	9Eh
ADCON0	1Fh	ADCON1	9Fh
	20h		A0h
General Purpose Register 96 Bytes	7Fh	General Purpose Register 80 Bytes	E8h
		accesses 70h-7Fh	F0h
			FFh
Bank 0	Bank 1	Bank 2	Bank 3
Indirect addr. ⁽¹⁾	100h	Indirect addr. ⁽¹⁾	130h
OPTION REG	101h	PCL	131h
PCL	102h	STATUS	132h
STATUS	103h	FSR	133h
FSR	104h	PORTB	134h
PORTB	105h		135h
PORTC	106h	TRISB	136h
PORTD ⁽¹⁾	107h		137h
PORTE ⁽¹⁾	108h		138h
PCLATH	109h		139h
INTCON	10Ah	INTCON	140h
EECON1	10Bh	EEDATA	141h
EECON2	10Dh	EEADDR	142h
Reserved ⁽²⁾	10Eh	EEDATH	143h
Reserved ⁽²⁾	10Fh	EEADRH	144h
	110h		145h
	111h		146h
	112h		147h
	113h		148h
	114h		149h
	115h		14Ah
	116h		14Bh
General Purpose Register 16 Bytes	117h	General Purpose Register 16 Bytes	14Ch
	118h		14Dh
	119h		14Eh
	11Ah		14Fh
	11Bh		14Ah
	11Ch		14Bh
	11Dh		14Ch
	11Eh		14Dh
	11Fh		14Eh
	120h		14Fh
General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	150h
			151h
accesses 70h-7Fh		accesses 70h-7Fh	152h
			153h
Bank 0	Bank 1	Bank 2	Bank 3
Indirect addr. ⁽¹⁾	154h	Indirect addr. ⁽¹⁾	154h
OPTION REG	155h	PCL	155h
PCL	156h	STATUS	156h
STATUS	157h	FSR	157h
FSR	158h	PORTB	158h
PORTB	159h		159h
PORTC	15Ah	TRISB	15Ah
PORTD ⁽¹⁾	15Bh		15Bh
PORTE ⁽¹⁾	15Ch		15Ch
PCLATH	15Dh		15Dh
INTCON	15Eh		15Eh
EECON1	15Fh		15Fh
EECON2	160h		160h
Reserved ⁽²⁾	161h		161h
Reserved ⁽²⁾	162h		162h
	163h		163h
	164h		164h
	165h		165h
	166h		166h
	167h		167h
	168h		168h
	169h		169h
	16Ah		16Ah
	16Bh		16Bh
	16Ch		16Ch
	16Dh		16Dh
	16Eh		16Eh
	16Fh		16Fh
	170h		170h
	171h		171h
	172h		172h
	173h		173h
	174h		174h
	175h		175h
	176h		176h
	177h		177h
	178h		178h
	179h		179h
	17Ah		17Ah
	17Bh		17Bh
	17Ch		17Ch
	17Dh		17Dh
	17Eh		17Eh
	17Fh		17Fh
	180h		180h
	181h		181h
	182h		182h
	183h		183h
	184h		184h
	185h		185h
	186h		186h
	187h		187h
	188h		188h
	189h		189h
	18Ah		18Ah
	18Bh		18Bh
	18Ch		18Ch
	18Dh		18Dh
	18Eh		18Eh
	18Fh		18Fh
	190h		190h
	191h		191h
	192h		192h
	193h		193h
	194h		194h
	195h		195h
	196h		196h
	197h		197h
	198h		198h
	199h		199h
	19Ah		19Ah
	19Bh		19Bh
	19Ch		19Ch
	19Dh		19Dh
	19Eh		19Eh
	19Fh		19Fh
	1A0h		1A0h
General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	150h
			151h
accesses 70h-7Fh		accesses 70h-7Fh	152h
			153h
Bank 0	Bank 1	Bank 2	Bank 3
Indirect addr. ⁽¹⁾	154h	Indirect addr. ⁽¹⁾	154h
OPTION REG	155h	PCL	155h
PCL	156h	STATUS	156h
STATUS	157h	FSR	157h
FSR	158h	PORTB	158h
PORTB	159h		159h
PORTC	15Ah	TRISB	15Ah
PORTD ⁽¹⁾	15Bh		15Bh
PORTE ⁽¹⁾	15Ch		15Ch
PCLATH	15Dh		15Dh
INTCON	15Eh		15Eh
EECON1	15Fh		15Fh
EECON2	160h		160h
Reserved ⁽²⁾	161h		161h
Reserved ⁽²⁾	162h		162h
	163h		163h
	164h		164h
	165h		165h
	166h		166h
	167h		167h
	168h		168h
	169h		169h
	16Ah		16Ah
	16Bh		16Bh
	16Ch		16Ch
	16Dh		16Dh
	16Eh		16Eh
	16Fh		16Fh
	170h		170h
	171h		171h
	172h		172h
	173h		173h
	174h		174h
	175h		175h
	176h		176h
	177h		177h
	178h		178h
	179h		179h
	17Ah		17Ah
	17Bh		17Bh
	17Ch		17Ch
	17Dh		17Dh
	17Eh		17Eh
	17Fh		17Fh
	180h		180h
	181h		181h
	182h		182h
	183h		183h
	184h		184h
	185h		185h
	186h		186h
	187h		187h
	188h		188h
	189h		189h
	18Ah		18Ah
	18Bh		18Bh
	18Ch		18Ch
	18Dh		18Dh
	18Eh		18Eh
	18Fh		18Fh
	190h		190h
	191h		191h
	192h		192h
	193h		193h
	194h		194h
	195h		195h
	196h		196h
	197h		197h
	198h		198h
	199h		199h
	19Ah		19Ah
	19Bh		19Bh
	19Ch		19Ch
	19Dh		19Dh
	19Eh		19Eh
	19Fh		19Fh
	1A0h		1A0h
General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	150h
			151h
accesses 70h-7Fh		accesses 70h-7Fh	152h
			153h
Bank 0	Bank 1	Bank 2	Bank 3
Indirect addr. ⁽¹⁾	154h	Indirect addr. ⁽¹⁾	154h
OPTION REG	155h	PCL	155h
PCL	156h	STATUS	156h
STATUS	157h	FSR	157h
FSR	158h	PORTB	158h
PORTB	159h		159h
PORTC	15Ah	TRISB	15Ah
PORTD ⁽¹⁾	15Bh		15Bh
PORTE ⁽¹⁾	15Ch		15Ch
PCLATH	15Dh		15Dh
INTCON	15Eh		15Eh
EECON1	15Fh		15Fh
EECON2	160h		160h
Reserved ⁽²⁾	161h		161h
Reserved ⁽²⁾	162h		162h
	163h		163h
	164h		164h
	165h		165h
	166h		166h
	167h		167h
	168h		168h
	169h		169h
	16Ah		16Ah
	16Bh		16Bh
	16Ch		16Ch
	16Dh		16Dh
	16Eh		16Eh
	16Fh		16Fh
	170h		170h
	171h		171h
	172h		172h
	173h		173h
	174h		174h
	175h		175h
	176h		176h
	177h		177h
	178h		178h
	179h		179h
	17Ah		17Ah
	17Bh		17Bh
	17Ch		17Ch
	17Dh		17Dh
	17Eh		17Eh
	17Fh		17Fh
	180h		180h
	181h		181h
	182h		182h
	183h		183h
	184h		184h
	185h		185h
	186h		186h
	187h		187h
	188h		188h
	189h		189h
	18Ah		18Ah
	18Bh		18Bh
	18Ch		18Ch
	18Dh		18Dh
	18Eh		18Eh
	18Fh		18Fh
	190h		190h
	191h		191h
	192h		192h
	193h		193h
	194h		194h
	195h		195h
	196h		196h
	197h		197h
	198h		198h
	199h		199h
	19Ah		19Ah
	19Bh		19Bh
	19Ch		19Ch
	19Dh		19Dh
	19Eh		19Eh
	19Fh		19Fh
	1A0h		1A0h
General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	150h
			151h
accesses 70h-7Fh		accesses 70h-7Fh	152h
			153h
Bank 0	Bank 1	Bank 2	Bank 3
Indirect addr. ⁽¹⁾	154h	Indirect addr. ⁽¹⁾	154h
OPTION REG	155h	PCL	155h
PCL	156h	STATUS	156h
STATUS	157h	FSR	157h
FSR	158h	PORTB	158h
PORTB	159h		159h
PORTC	15Ah	TRISB	15Ah
PORTD ⁽¹⁾	15Bh		15Bh
PORTE ⁽¹⁾	15Ch		15Ch
PCLATH	15Dh		15Dh
INTCON	15Eh		15Eh
EECON1	15Fh		15Fh
EECON2	160h		160h
Reserved ⁽²⁾	161h		161h
Reserved ⁽²⁾	162h		162h
	163h		163h
	164h		164h
	165h		165h
	166h		166h
	167h		167h
	168h		168h
	169h		169h
	16Ah		16Ah
	16Bh		16Bh
	16Ch		16Ch
	16Dh		16Dh
	16Eh		16Eh
	16Fh		16Fh
	170h		170h
	171h		171h
	172h		172h
	173h		173h
	174h		174h
	175h		175h
	176h		176h
	177h		177h
	178h		178h
	179h		179h
	17Ah		17Ah
	17Bh		17Bh
	17Ch		17Ch
	17Dh		17Dh
	17Eh		17Eh
	17Fh		17Fh
	180h		180h
	181h		181h
	182h		182h
	183h		183h
	184h		184h
	185h		185h
	186h		186h
	187h		187h
	188h		188h
	189h		189h
	18Ah		18Ah
	18Bh		18Bh
	18Ch		18Ch
	18Dh		18Dh
	18Eh		18Eh

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 KOD MP : DEK 3133

RUJUKAN II

PIC16F87XA

TABLE 15-2: PIC16F87XA INSTRUCTION SET

Mnemonic. Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECf	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add Literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND Literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call Subroutine	2	10 0kkk kkkk kkkk		
CLRWD	-	Clear Watchdog Timer	1	00 0000 0110 0100	TO,PD	
GOTO	k	Go to Address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR Literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move Literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from Interrupt	2	00 0000 0000 1001		
RETLW	k	Return with Literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000	TO,PD	
SLEEP	-	Go into Standby mode	1	00 0000 0110 0011		
SUBLW	k	Subtract W from Literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR Literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMRO register (and where appl cable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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RUJUKAN III**Reference for MikroC functions:**

Functions	Using C Function samples
Initialize LCD to PORTD	Lcd_Init(&PORTD);
Clear LCD	Lcd_Cmd(Lcd_CLEAR)
Read ADC conversion at AN0	Adc_Read(0)
Convert floating value to String	Unsigned float ABC; //variable ABC as float Char CBA[13]; //variable CBA with 13 character long ABC = 123.456; FloatToStr(ABC, CBA); //CBA = “123.456” (string format)
Show text in LCD screen	Lcd_Out(2,1, “Hello”); // Show text “Hello” at Line 2 column 1
Configure Analog inputs with Vref using Internal Vref +5V.	ADCON1 = 0x80;
Initialize PWM Freq.	Pwm_Init(unsigned long freq)
PWM Change Duty Cycle to 75%	DutyCycle = 75/100 * 255 = 191 Pwm_Change_Duty(191);
Enable PMW	Pwm_Start();
Receive Usart data	int a = Usart_Read();
Transmit Usart data	int a = 100; Usart_Write(a);

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RUJUKAN IV**Special Function Registers****INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMROIE	INTE	RBIE	TMROIF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE**: Global Interrupt Enable bit

1 = Enables all unmasked interrupts

0 = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit

1 = Enables all unmasked peripheral interrupts

0 = Disables all peripheral interrupts

bit 5 **TMROIE**: TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 interrupt

0 = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit

1 = Enables the RB0/INT external interrupt

0 = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt

0 = Disables the RB port change interrupt

bit 2 **TMROIF**: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)

0 = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit

1 = The RB0/INT external interrupt occurred (must be cleared in software)

0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set

the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared
 (must be cleared in software).

0 = None of the RB7:RB4 pins have changed state

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KOD MP : DEK 3133**RUJUKAN V****OPTION_REG REGISTER (ADDRESS 81h, 181h)**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0
bit 7							

RBPU: PORTB Pull-up Enable bit

1 = PORTB pull-ups are disabled

0 = PORTB pull-ups are enabled by individual port latch values

bit 6 INTEDG: Interrupt Edge Select bit

1 = Interrupt on rising edge of RB0/INT pin

0 = Interrupt on falling edge of RB0/INT pin

bit 5 TOCS: TMR0 Clock Source Select bit

1 = Transition on RA4/T0CKI pin

0 = Internal instruction cycle clock (CLKO)

bit 4 TOSE: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on RA4/T0CKI pin

0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 PSA: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

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RUJUKAN VI

REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7

ADFM: A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6

ADCS2: A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in bold)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	Frc (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	Frc (clock derived from the internal A/D RC oscillator)

bit 5-4 Unimplemented: Read as '0'

bit 3-0 PCFG3:PCFG0: A/D Port Configuration Control bits

PCFG <3:0>	ANT	ANG	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF-	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF-	A	A	A	AN3	VSS	4/1
0100	D	D	D	C	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	C	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	8/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF-	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF-	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	C	VREF-	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references