# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## PEPERIKSAAN AKHIR
## SEMESTER I
## SESI 2009/2010

| | | |
|---|---|---|
| NAMA MATAPELAJARAN | : | MIKROPENGAWAL |
| KOD MATAPELAJARAN | : | DEK 3133 |
| KURSUS | : | 3 DET, DEE |
| TARIKH PEPERIKSAAN | : | NOVEMBER 2009 |
| JANGKAMASA | : | 3 JAM |
| ARAHAN | : | JAWAB **SEMUA** SOALAN |

KERTAS SOALAN INI MENGANDUNGI TUJUH BELAS (17) MUKA SURAT

**SOALAN DALAM BAHASA MALAYSIA**

**BAHAGIAN A**

**S1** (a) Nyatakan **definisi** bagi *Microcontroller* dan berikan empat (**4**) **perkara** yang perlu diberi perhatian untuk memilih *Microcontroller* yang sesuai
(5 markah)

(b) Rajah S1(b) adalah struktur ingatan sebuah Mikropengawal. Terdapat 8 talian data dan 12 talian alamat yang dihubungkan antara CPU dan ingatan. Dengan mengambil kira 1Kb adalah bersamaan 1024byte.

(i) Kirakan saiz ruangan ingatan tersebut.
(ii) Apakah jenis talian bas yang akan menentukan saiz ingatan sebuah Mikropengwal.
(4 markah)

(c) Kira jumlah kitar suruhan bagi turutan suruhan di bawah.

```
Delay  MOVLW 0xFF
       MOVWF timer
       NOP
       NOP
Down   DECFSZ timer
       GOTO   down
       RETURN
```

(5 markah)

(d) Sekiranya anda menggunakan pemasa *TMR0* bersama pengayun berkelajuan 20MHz dan *Prescaler* 1:256, **kirakan masa** yang diperlukan untuk *TMRO* menghasilkan satu (1) limpahan (0-255).
(5 markah)

(e) PIC16F877A menggunakan bekalan jam berfrekuensi 40MHz. **Tunjukkan pengiraan** untuk mengetahui tempoh masa yang diambil oleh Mikropengawal menyelesaikan satu (1) suruhan dan **berapakah** suruhan yang mampu dilaksanakan oleh Mikropengawal dalam tempoh 5.0μs dan 125.0 μs?
(6 markah)

**S2** (a) PIC16F877A mempunyai resolusi 10-Bit (0b1111111111=1023) bagi penukaran analog kepada digital. Voltan rujukan adalah 3V, dapatkan nilai **Saiz Langkah** dan **Keluaran Digital** bagi *ADC* tersebut sekiranya voltan masukan analog adalah 1.23V. Berikan jawapan dalam nombor binari mengikut turutan *bit*.

(8 markah)

(b) **Berikan arahan** *MikroC* yang sesuai untuk:

(i) Proses menyimpan data pada ingatan *EEPROM*.
(ii) Melakukan konfigurasi *LCD* pada *PORTB*.
(iii) Mencetak perkataan DEK3133 pada paparan *LCD* di kedudukan baris 2 dan lajur 2.

(6 markah)

(c) Rajah S2(c) menunjukkan dua Mikropengawal yang berhubung antara satu sama lain dengan menggunakan modul perkakasan *USART*. **Berikan arahan** *MikroC* yang membolehkan Mikropengawal A **menyalakan kesemua LED** pada Mikropengawal B. Kelajuan penghantaran yang digunakan adalah 9600 *bit/s*. Tulis kod aturcara bagi kedua-dua Mikropengawal.

(7 markah)

(d) Merujuk pada Rajah S2(d), sebuah LED disambung kepada modul *PWM* pada frekuensi 5Khz. **Berikan arahan** *MikroC* supaya nyalaan LED tersebut adalah kurang 50 peratus daripada kecerahan asalnya.

(4 markah)

## BAHAGIAN B

**S3** Rajah S3 menunjukkan sebuah system kawalan untuk mengekalkan suhu sebuah bilik pada tahap 30°C hingga 40°C. Sistem ini menggunakan penderia suhu yang mengukur suhu di antara 0°C - 100°C. Keluaran litar penderia suhu adalah voltan analog (0V-5V) yang merupakan masukan kepada litar PIC. Terdapat dua komponen LED yang berfungsi untuk menunjukkan tahap suhu semasa (D2:normal dan D1:panas) dan sebuah komponen kipas yang berfungsi untuk menyejukkan suhu bilik sekiranya suhu tertentu dicapai. LED dan kipas akan berfungsi berdasarkan Jadual S3. Voltan rujukan PIC adalah 5V.

(a) Dapatkan :

(i) Saiz Langkah.
(ii) **Nilai ADC** apabila nilai $V_{in}$ pada AN0 adalah 3V.
(i) **Nilai suhu** dalam *Celsius* sekiranya $V_{in}$ = 2V

(5 markah)

(b) Sekiranya PIC menggunakan Voltan rujukan +5V, **tuliskan aturcara** *MikroC* yang menunjukkan proses penukaran analog kepada digital dan seterusnya mengawal suhu bilik.

(20 markah)

**S4** Litar dalam Rajah S4 beroperasi dengan memaparkan nilai pengiraan secara menaik bermula dari nombor 0 hingga 9 dengan sela masa 1 saat. Pemasa lengahan PIC adalah daripada pemasa TMR0 dengan skala 1:64 dan nilai awalan TMR0 adalah 131. Sekiranya PIC dibekalkan pengayun (***Fosc)*** dengan frekuensi 4Mhz,

(a) Dapatkan:

(i) **Tempoh masa** bagi limpahan TMR0 bermula dari 131 hingga 255.
(ii) **Bilangan limpahan** TMR0 yang diperlukan untuk mendapatkan tempoh lengah satu (1) saat.

(5 markah)

(b) Dengan menggunakan pemasa TMR0 **binakan kod pengaturcaraan *C*** di mana paparan *Seven Segment* akan memaparkan nilai pengiraan bermula dari 0 hingga 9 dengan sela masa 1 saat. Gunakan jadual S4(b) untuk nilai-nilai binari *Seven Segment.*

(20 markah)

**SOALAN DALAM BAHASA INGGERIS**

**PART A**

**Q1** (a) Give definition of Microcontroller and give four (4) important aspects required attention to choose suitable Microcontroller.

(4 marks)

(b) Figure Q1(b) shows the memory structure of microcontroller. There are 8 data buses and 12 address buses connected between CPU and memory. Considering 1Kb is equal to 1024bytes:

(i) Calculate the size of the memory for thus microcontroller.
(ii) What type of buses will determine the memory size of the microcontroller?

(4 marks)

(c) Base on the assembly language below, calculate the total cycle of the instructions.

```
Delay  MOVLW 0xFF
       MOVWF timer
       NOP
       NOP
Down   DECFSZ timer
       GOTO  down
       RETURN
```

(5 marks)

(d) If you use TMR0 timer with 20MHz Oscillator and Prescaler 1:256, **calculate the time required** for TMR0 to produce one (1) Overflow (0 to 255)

(5 marks)

(e) A PIC16F877A uses a clock frequency of 40MHz. **Show the calculation** to know a time period taken by Microcontroller to complete one (1) instruction and **how many Instructions** can be executed by microcontroller within 5.0μs and 125.0μs?

(6 marks)

**Q2** (a) A PIC16F877A has 10-Bit resolutions (0b1111111111=1023) for analog to digital conversion (ADC). By using the voltage reference of 5V, find the **Step Size** and **Digital Output** of ADC when the analog input is 1.23V. Give your answer in binary format by following the bit order.

(8 marks)

(b) Give **suitable *MikroC* instruction** for:
(i) Write a data to EEPROM.
(ii) Configure LCD to be used at PORTB.
(iii) Print word DEK3133 on LCD screen at row 2 and column 2.

(6 marks)

(c) Figure S2 (c) are two Microcontroller interconnect between each other using the USART module hardware. Give the instructions of *MikroC* that allows the Microcontroller A to lit on all LED at Microcontroller B. Speed transmission used is 9600 bits/s. Write your code for both microcontroller.

(7 marks)

(d) Refer to Figure S2 (d), an LED is connected to the PWM module at frequency 5Khz. Give the instructions of *MikroC* to switch on the LED about 50 percent of its original brightness.

(4 marks)

**PART B**

**Q3** Figure Q3 shows a control system to maintain room temperature between 30°C to 40°C. The system is used a temperature sensor to measure the temperature between 0°C to 100°C. The output of temperature sensor is analog voltage (0V-5V) which is the input to the PIC circuit. There are two LED components which work as indicator for the current temperatures level (D2: normal and DI: hot) and a fan component which operate to cool down the room temperature when a certain temperature is achieved. LEDs and fan will functioned based on Table S3. Voltage reference used by PIC is 5V.

(a) Find:
(i) **Step size**.
(ii) **ADC result** when $V_{in}$ to AN0 is 3V.
(iii) **Temperature Value** in degree celsius when $V_{in}$ = 2V.
(5 marks)

(b) If the PIC uses voltage reference of +5V, **write a C program** to show the conversion process from analog to digital and then control the room temperature.
(20 marks)

**Q4** Circuit in Figure Q4 operates by showing the counter value by rising up the number value beginning from 0 to 9 with time interval 1 second. Delay Timer PIC is from Hardware Timer (TMR0) with prescaler 1:64 and preload value TMR0 is set to 131. If the PIC is provided with Oscillator frequency (Fosc) 4 MHz,

(a) Determine:

(i) **Time taken** for TMRO to overflow starting from 131 to 255.
(ii) Number of TMR0 **overflows required** to get 1 second delay.
(5 marks)

(b) By using the TMR0 Timer **write a *C* program** where the Seven Segment display will show counting value from 0 to 9 with time interval 1 second. Use the Table S4 (b) for Seven Segment binary number.
(20 marks)

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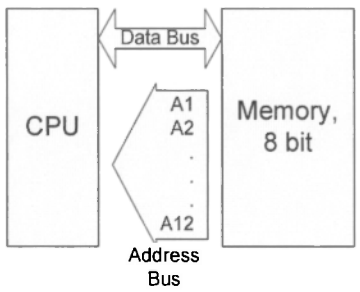
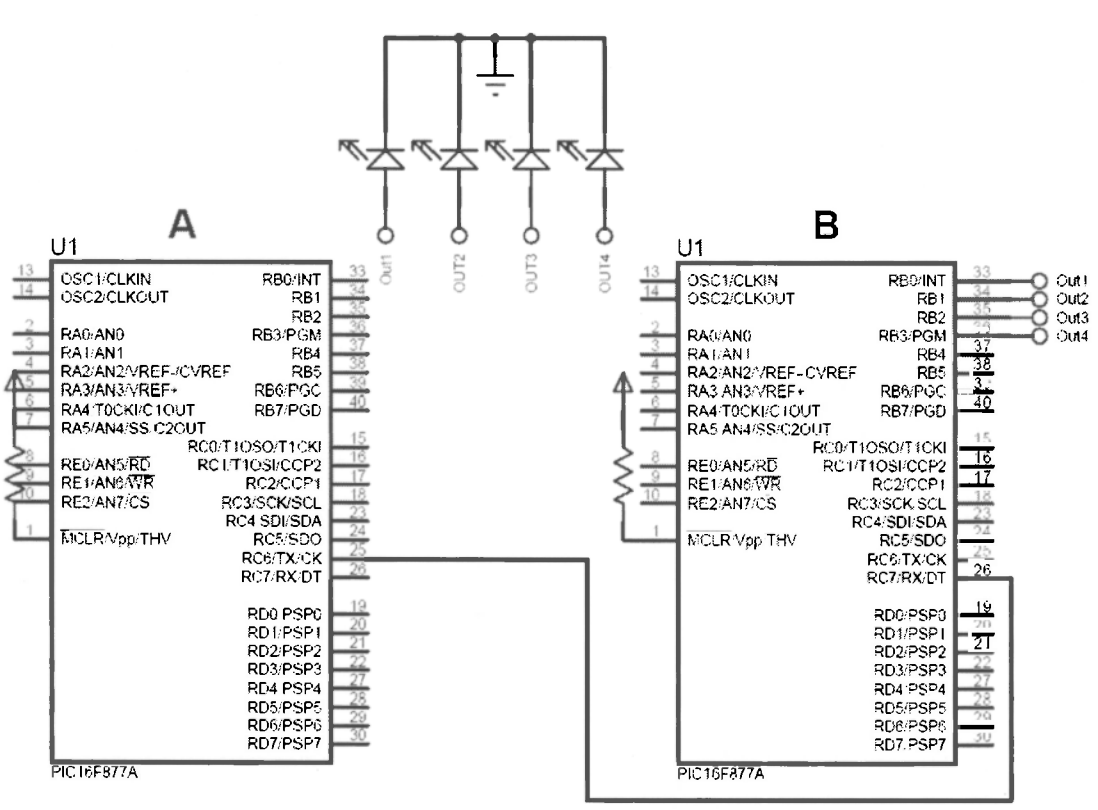
KOD MP : DEK 3133




**Rajah S1(b) / Figure Q1(b)**




**Rajah S2(c) / Figure Q2(c)**

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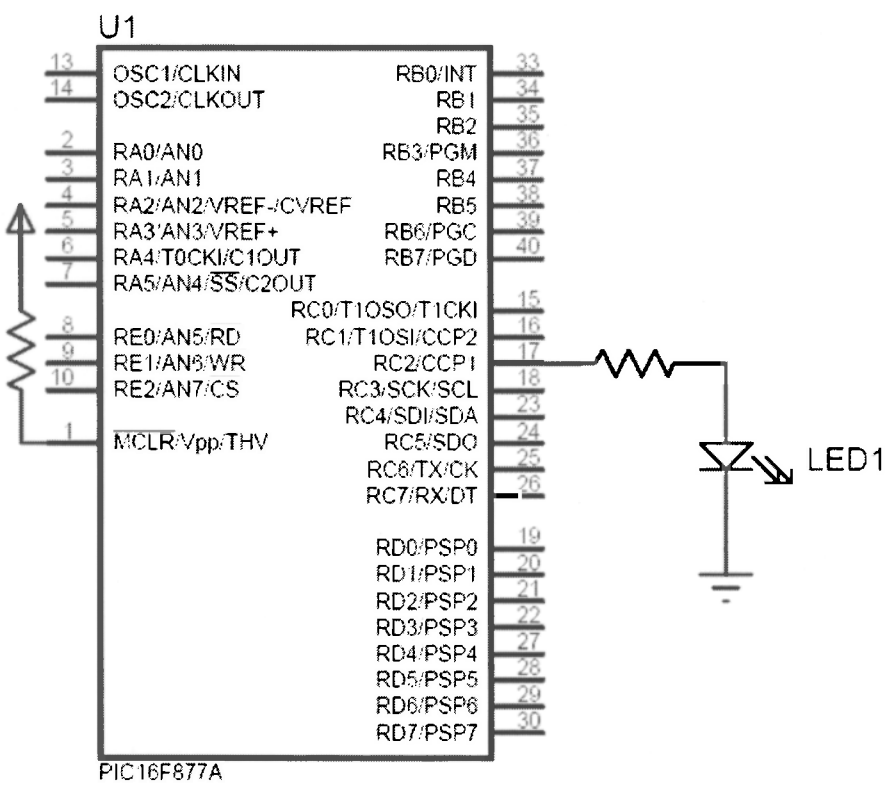
KOD MP : DEK 3133




**Rajah S2(d) / Figure Q2(d)**

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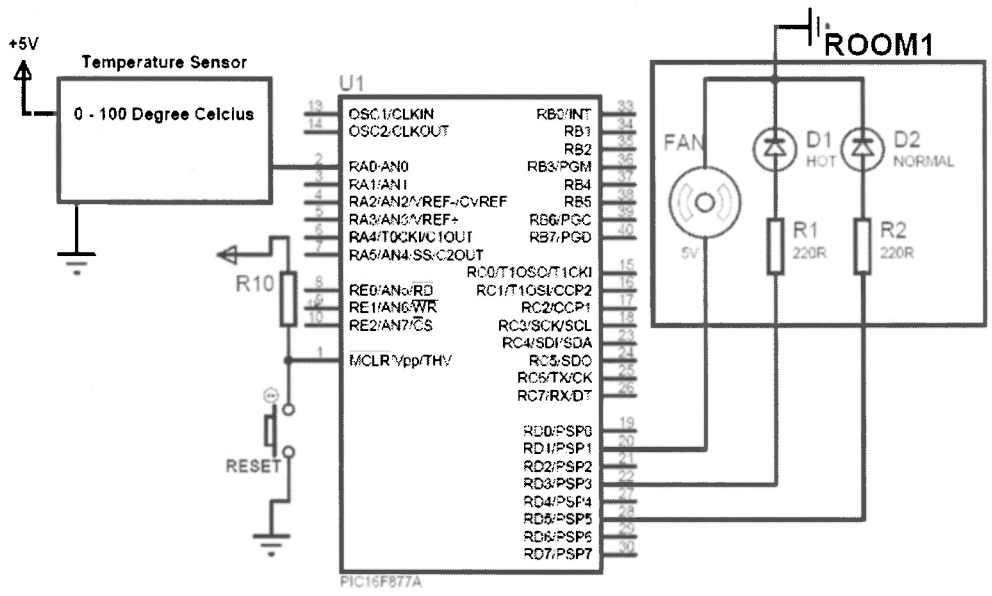
MATAPELAJARAN : MIKROPENGAWAL

KURSUS : 3 DET,DEE
KOD MP : DEK 3133




**Rajah S3 / Figure Q3**

| Temperatures | LED and Fan Status |
|---|---|
| Above 39°C | Fan = Rotate (Fan is rotate and stop when reach at 30°C) |
| Above 35 °C | LED D1(Hot) = ONN<br>LED D2(Normal) = OFF |
| Below 35°C | LED D1(Hot) = OFF<br>LED D2(Normal) = ON |
| Below 30°C | Fan = Stop |

**Jadual S3 / Table Q3**

**PEPERIKSAAN AKHIR**

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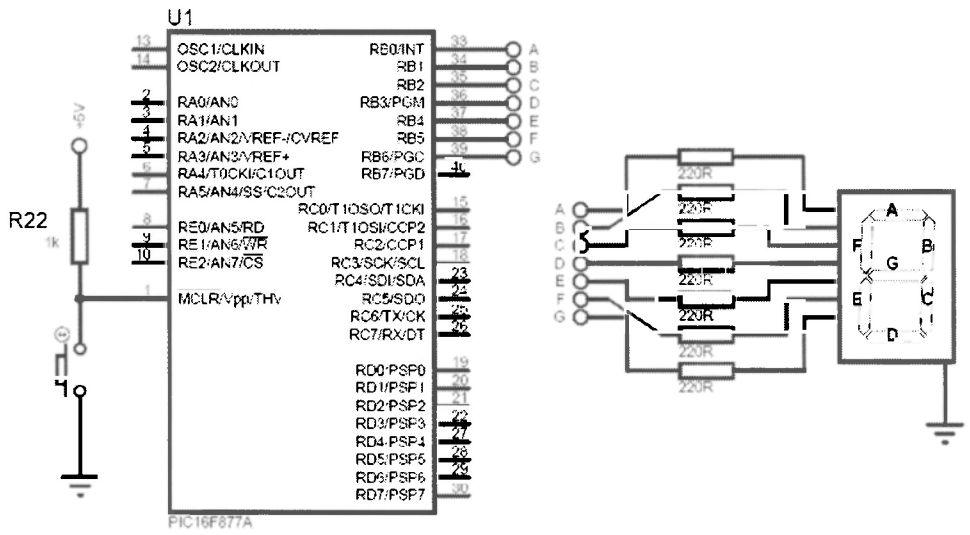
KURSUS : 3 DET,DEE
KOD MP : DEK 3133




**Rajah S4 / Figure Q4**

| Seven Segment No. | Binary value |
|---|---|
| 9 | 01101111 |
| 8 | 01111111 |
| 7 | 00000111 |
| 6 | 01111101 |
| 5 | 01101101 |
| 4 | 01100110 |
| 3 | 01001111 |
| 2 | 01011011 |
| 1 | 00000110 |
| 0 | 00111111 |

**Jadual S4 (b) / Table Q4 (b)**

## PEPERIKSAAN AKHIR

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## RUJUKAN I

FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP

| Bank 0 | File Address | Bank 1 | File Address | Bank 2 | File Address | Bank 3 | File Address |
|---|---|---|---|---|---|---|---|
| Indirect addr.(*) | 00h | Indirect addr.(*) | 80h | Indirect addr.(*) | 100h | Indirect addr.(*) | 180h |
| TMR0 | 01h | OPTION_REG | 81h | TMR0 | 101h | OPTION_REG | 181h |
| PCL | 02h | PCL | 82h | PCL | 102h | PCL | 182h |
| STATUS | 03h | STATUS | 83h | STATUS | 103h | STATUS | 183h |
| FSR | 04h | FSR | 84h | FSR | 104h | FSR | 184h |
| PORTA | 05h | TRISA | 85h | | 105h | | 185h |
| PORTB | 06h | TRISB | 86h | PORTB | 106h | TRISB | 186h |
| PORTC | 07h | TRISC | 87h | | 107h | | 187h |
| PORTD(1) | 08h | TRISD(1) | 88h | | 108h | | 188h |
| PORTE(1) | 09h | TRISE(1) | 89h | | 109h | | 189h |
| PCLATH | 0Ah | PCLATH | 8Ah | PCLATH | 10Ah | PCLATH | 18Ah |
| INTCON | 0Bh | INTCON | 8Bh | INTCON | 10Bh | INTCON | 18Bh |
| PIR1 | 0Ch | PIE1 | 8Ch | EEDATA | 10Ch | EECON1 | 18Ch |
| PIR2 | 0Dh | PIE2 | 8Dh | EEADR | 10Dh | EECON2 | 18Dh |
| TMR1L | 0Eh | PCON | 8Eh | EEDATH | 10Eh | Reserved(2) | 18Eh |
| TMR1H | 0Fh | | 8Fh | EEADRH | 10Fh | Reserved(2) | 18Fh |
| T1CON | 10h | | 90h | | 110h | | 190h |
| TMR2 | 11h | SSPCON2 | 91h | | 111h | | 191h |
| T2CON | 12h | PR2 | 92h | | 112h | | 192h |
| SSPBUF | 13h | SSPADD | 93h | | 113h | | 193h |
| SSPCON | 14h | SSPSTAT | 94h | | 114h | | 194h |
| CCPR1L | 15h | | 95h | | 115h | | 195h |
| CCPR1H | 16h | | 96h | | 116h | | 196h |
| CCP1CON | 17h | | 97h | General Purpose Register 16 Bytes | 117h | General Purpose Register 16 Bytes | 197h |
| RCSTA | 18h | TXSTA | 98h | | 118h | | 198h |
| TXREG | 19h | SPBRG | 99h | | 119h | | 199h |
| RCREG | 1Ah | | 9Ah | | 11Ah | | 19Ah |
| CCPR2L | 1Bh | | 9Bh | | 11Bh | | 19Bh |
| CCPR2H | 1Ch | CMCON | 9Ch | | 11Ch | | 19Ch |
| CCP2CON | 1Dh | CVRCON | 9Dh | | 11Dh | | 19Dh |
| ADRESH | 1Eh | ADRESL | 9Eh | | 11Eh | | 19Eh |
| ADCON0 | 1Fh | ADCON1 | 9Fh | | 11Fh | | 19Fh |
| General Purpose Register 96 Bytes | 20h | General Purpose Register 80 Bytes | A0h | General Purpose Register 80 Bytes | 120h | General Purpose Register 80 Bytes | 1A0h |
| | 7Fh | | EFh | | 16Fh | | 1EFh |
| | | accesses 70h-7Fh | F0h | accesses 70h-7Fh | 170h | accesses 70h - 7Fh | 1F0h |
| | | | FFh | | 17Fh | | 1FFh |

☐ Unimplemented data memory locations, read as '0'.
* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876A.
2: These registers are reserved; maintain these registers clear.

**PEPERIKSAAN AKHIR**

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**RUJUKAN II**

# PIC16F87XA

**TABLE 15-2: PIC16F87XA INSTRUCTION SET**

| Mnemonic, Operands | | Description | Cycles | 14-Bit Opcode MSb LSb | Status Affected | Notes |
|---|---|---|---|---|---|---|
| **BYTE-ORIENTED FILE REGISTER OPERATIONS** | | | | | | |
| ADDWF | f, d | Add W and f | 1 | 00 0111 dfff ffff | C,DC,Z | 1,2 |
| ANDWF | f, d | AND W with f | 1 | 00 0101 dfff ffff | Z | 1,2 |
| CLRF | f | Clear f | 1 | 00 0001 1fff ffff | Z | 2 |
| CLRW | - | Clear W | 1 | 00 0001 0xxx xxxx | Z | |
| COMF | f, d | Complement f | 1 | 00 1001 dfff ffff | Z | 1,2 |
| DECF | f, d | Decrement f | 1 | 00 0011 dfff ffff | Z | 1,2 |
| DECFSZ | f, d | Decrement f, Skip if 0 | 1(2) | 00 1011 dfff ffff | | 1,2,3 |
| INCF | f, d | Increment f | 1 | 00 1010 dfff ffff | Z | 1,2 |
| INCFSZ | f, d | Increment f, Skip if 0 | 1(2) | 00 1111 dfff ffff | | 1,2,3 |
| IORWF | f, d | Inclusive OR W with f | 1 | 00 0100 dfff ffff | Z | 1,2 |
| MOVF | f, d | Move f | 1 | 00 1000 dfff ffff | Z | 1,2 |
| MOVWF | f | Move W to f | 1 | 00 0000 1fff ffff | | |
| NOP | - | No Operation | 1 | 00 0000 0xx0 0000 | | |
| RLF | f, d | Rotate Left f through Carry | 1 | 00 1101 dfff ffff | C | 1,2 |
| RRF | f, d | Rotate Right f through Carry | 1 | 00 1100 dfff ffff | C | 1,2 |
| SUBWF | f, d | Subtract W from f | 1 | 00 0010 dfff ffff | C,DC,Z | 1,2 |
| SWAPF | f, d | Swap nibbles in f | 1 | 00 1110 dfff ffff | | 1,2 |
| XORWF | f, d | Exclusive OR W with f | 1 | 00 0110 dfff ffff | Z | 1,2 |
| **BIT-ORIENTED FILE REGISTER OPERATIONS** | | | | | | |
| BCF | f, b | Bit Clear f | 1 | 01 00bb bfff ffff | | 1,2 |
| BSF | f, b | Bit Set f | 1 | 01 01bb bfff ffff | | 1,2 |
| BTFSC | f, b | Bit Test f, Skip if Clear | 1 (2) | 01 10bb bfff ffff | | 3 |
| BTFSS | f, b | Bit Test f, Skip if Set | 1 (2) | 01 11bb bfff ffff | | 3 |
| **LITERAL AND CONTROL OPERATIONS** | | | | | | |
| ADDLW | k | Add Literal and W | 1 | 11 111x kkkk kkkk | C,DC,Z | |
| ANDLW | k | AND Literal with W | 1 | 11 1001 kkkk kkkk | Z | |
| CALL | k | Call Subroutine | 2 | 10 0kkk kkkk kkkk | | |
| CLRWDT | - | Clear Watchdog Timer | 1 | 00 0000 0110 0100 | TO,PD | |
| GOTO | k | Go to Address | 2 | 10 1kkk kkkk kkkk | | |
| IORLW | k | Inclusive OR Literal with W | 1 | 11 1000 kkkk kkkk | Z | |
| MOVLW | k | Move Literal to W | 1 | 11 00xx kkkk kkkk | | |
| RETFIE | - | Return from Interrupt | 2 | 00 0000 0000 1001 | | |
| RETLW | k | Return with Literal in W | 2 | 11 01xx kkkk kkkk | | |
| RETURN | - | Return from Subroutine | 2 | 00 0000 0000 1000 | | |
| SLEEP | - | Go into Standby mode | 1 | 00 0000 0110 0011 | TO,PD | |
| SUBLW | k | Subtract W from Literal | 1 | 11 110x kkkk kkkk | C,DC,Z | |
| XORLW | k | Exclusive OR Literal with W | 1 | 11 1010 kkkk kkkk | Z | |

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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**RUJUKAN III**

**Reference for MikroC functions:**

| Functions | Using C Function samples |
|---|---|
| Initialize LCD to PORTD | Lcd_Init(&PORTD); |
| Clear LCD | Lcd_Cmd(Lcd_CLEAR) |
| Read ADC conversion at AN0 | Adc_Read(0) |
| Convert floating value to String | Unsigned float ABC; //variable ABC as float<br>Char CBA[13]; //variable CBA with 13 character long<br>ABC = 123.456;<br>FloatToStr(ABC, CBA); //CBA = "123.456" (string format) |
| Show text in LCD screen | Lcd_Out(2,1, "Hello"); // Show text "Hello" at Line 2 column 1 |
| Configure Analog inputs with Vref using Internal Vref +5V. | ADCON1 = 0x80; |
| Initialize PWM Freq. | Pwm_Init(unsigned long freq) |
| PWM Change Duty Cycle to 75% | DutyCycle = 75/100 * 255 = 191<br>Pwm_Change_Duty(191); |
| Enable PMW | Pwm_Start(); |
| Receive Usart data | int a = Usart_Read(); |
| Transmit Usart data | int a = 100; Usart_Write(a); |

**PEPERIKSAAN AKHIR**

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**RUJUKAN IV**

## Special Function Registers

INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | TMR0IE | INTE | RBIE | TMR0IF | INTF | RBIF |
| bit 7 | | | | | | | bit 0 |

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts
bit 6 **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
bit 5 **TMR0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt
bit 4 **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt
bit 3 **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
bit 2 **TMR0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
bit 1 **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur
bit 0 **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set
the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared
(must be cleared in software).
0 = None of the RB7:RB4 pins have changed state

**PEPERIKSAAN AKHIR**

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**RUJUKAN V**

**OPTION_REG REGISTER (ADDRESS 81h, 181h)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

**RBPU:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values
bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin
bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKO)
bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin
bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
**PS2:PS0**: Prescaler Rate Select bits

| Bit Value | TMR0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

## PEPERIKSAAN AKHIR

SEMESTER/SESI : SEMESTER 1/2009/10
MATAPELAJARAN : MIKROPENGAWAL

KURSUS : 3 DET,DEE
KOD MP : DEK 3133

## RUJUKAN VI

**REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)**

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | ADCS2 | — | — | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in bold)

| ADCON1 <ADCS2> | ADCON0 <ADCS1:ADCS0> | Clock Conversion |
|---|---|---|
| **0** | 00 | Fosc/2 |
| **0** | 01 | Fosc/8 |
| **0** | 10 | Fosc/32 |
| **0** | 11 | FRC (clock derived from the internal A/D RC oscillator) |
| **1** | 00 | Fosc/4 |
| **1** | 01 | Fosc/16 |
| **1** | 10 | Fosc/64 |
| **1** | 11 | FRC (clock derived from the internal A/D RC oscillator) |

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

| PCFG <3:0> | AN7 | AN6 | AN5 | AN4 | AN3 | AN2 | AN1 | AN0 | VREF+ | VREF- | C/R |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | A | A | A | A | A | A | A | A | VDD | VSS | 8/0 |
| 0001 | A | A | A | A | VREF- | A | A | A | AN3 | VSS | 7/1 |
| 0010 | D | D | D | A | A | A | A | A | VDD | VSS | 5/0 |
| 0011 | D | D | D | A | VREF- | A | A | A | AN3 | VSS | 4/1 |
| 0100 | D | D | D | D | A | D | A | A | VDD | VSS | 3/0 |
| 0101 | D | D | D | D | VREF- | D | A | A | AN3 | VSS | 2/1 |
| 011x | D | D | D | D | D | D | D | D | — | — | 0/0 |
| 1000 | A | A | A | A | VREF- | VREF- | A | A | AN3 | AN2 | 6/2 |
| 1001 | D | D | A | A | A | A | A | A | VDD | VSS | 6/0 |
| 1010 | D | D | A | A | VREF- | A | A | A | AN3 | VSS | 5/1 |
| 1011 | D | D | A | A | VREF- | VREF- | A | A | AN3 | AN2 | 4/2 |
| 1100 | D | D | D | A | VREF- | VREF- | A | A | AN3 | AN2 | 3/2 |
| 1101 | D | D | D | D | VREF- | VREF- | A | A | AN3 | AN2 | 2/2 |
| 1110 | D | D | D | D | D | D | D | A | VDD | VSS | 1/0 |
| 1111 | D | D | D | D | VREF- | VREF- | D | A | AN3 | AN2 | 1/2 |

A = Analog input D = Digital I/O
C/R = # of analog input channels/# of A/D voltage references