



**UNIVERSITI TUN HUSSEIN ONN  
MALAYSIA**

**FINAL EXAMINATION  
SEMESTER I  
SESSION 2009/2010**

SUBJECT NAMA : ELECTRONIC DIGIT  
SUBJECT CODE : DEE 2123  
COURSE : 2 DET / DEE / DEX  
EXAMINATION DATE : NOVEMBER 2009  
DURATION : 2 ½ HOURS  
INSTRUCTION : **PART A: ANSWER ALL QUESTIONS**  
**PART B: ANSWER THREE (3)**  
**QUESTIONS OUT OF FIVE (5)**  
**QUESTIONS**

**THIS PAPER CONSIST OF 11 PAGES**

**PART A** (Show all steps)

- Q1**
- (a) Express the number 137.05 as a sum of product by multiplying each digit by its appropriate weight. (2 marks)
  - (b) Multiply the binary numbers 1011 and 1111. (2 marks)
  - (c) Add the BCD numbers 147 and 75. (2 marks)
- Q2**
- (a) Find the 2's complement of the number -29. (2 marks)
  - (b) Using 2's complement number method add the numbers - 22 and -11. (2 marks)
  - (c) Convert the Gray code 10101111 to binary number. (2 marks)
- Q3**
- (a) Prove that  $A + A'B = A + B$ . (2 marks)
  - (b) Sketch the output waveform X for an exclusive-OR gate with the given input waveforms A and B shown in Figure Q3 (b) (2 marks)
  - (c) Draw the distinctive shape how an AND gate can be produced from a combination of the NOR gates only? (2 marks)

- Q4** (a) Simplify the expression  $A'BC' + A'BC + ABC'$  (2 marks)
- (b) Apply the De Morgan's theorem, to solve the expression  $\overline{M'N LN' (LMIN)}$  (2 marks)
- (c) Write the Boolean equation at each output stage for the circuit shown in Figure Q4(c). Use De Morgan's theorem and Boolean algebra rules to simplify the output expression at C. (2 marks)
- Q5** (a) By using the truth table method, convert the non standard expression of  $A' + AB' + AB'C$  into the standard SOP form. (4 marks)
- (b) Map the Boolean expression  $A'B'C' + A'B'C + A'BC' + ABC + AB'C' + AB'C$  into the Karnaugh map (2 marks)
- (c) From your answer in Q5 (b) above, group the cell contents to get the simplest Boolean expression. (4 marks)
- Q6** (a) From the half adder truth table:
- i) Derive the expression for Cout and SUM (2 marks)
- ii) From your expression in Q6 (a) (i), draw the logic diagram for the half adder. (2 marks)
- (b) Figure Q6 (b) show the incomplete connection and data for a 3 bits parallel adder. Complete the given figure to show the correct connection and correct data location and the sum and intermediate carries when the binary numbers 110 and 101 are being added. (2 marks)

**PART B** (Show all steps)**Q7** Examine the circuit given in Figure Q7.

- (a) By assuming no voltage drop across the resistor, the voltage +5V will give the input as HIGH, and ground as LOW, complete the given table for input and output for the switching conditions as given in the table. (5 marks)
- (b) Write the Boolean expression for the output at each gate. Obtain the simplest expression for the output Z (5 marks)
- (c) Map the data for output Z, into Karnaugh Map. Regroup the cells and get the simplified expression for POS and SOP. (5 marks)
- (d) Using both your simplified expression, draw the logic gate. (5 marks)

- Q8** (a) Convert the decimal number +13 into its sign magnitude number. (2 marks)
- (b) Using repeat division method, convert the decimal number 48 to binary number. (2 marks)
- (c) Perform the division of 100110 with 11 (3 marks)
- (d) Using the 2's complement number system and eight bit binary add the numbers - 64 with -20. (3 marks)
- (e) Convert the hexadecimal number B4F to decimal number (3 marks)
- (f) Convert the decimal number 137 to binary number and to BCD number. What can you say between binary number and BCD number? (4 marks)
- (g) Add the BCD numbers 59 and 38. (3 marks)

- Q9** (a) Using mathematical method, convert the Boolean expression  $(K+L')(M+N')$  into standard POS form. (5 marks)
- (b) Using mathematical method, convert the Boolean expression  $PQ+R'S+Q'$  into its standard form. (5 marks)
- (c) Map the Boolean expression  $(B+C+D)(A+B+C'+D)(A'+B+C+D')(A+B'+C+D)(A'+B'+C+D)$  into a Karnaugh map. From your Karnaugh map, group the cell contents and get the minimum expression for SOP and POS. (10 marks)
- Q10** (a) Figure Q10 (a) shows a logic symbol and data selection for a 1 of 4 multiplexer. The data output is equal to  $D_0$  only if  $S_1=0$  and  $S_0=0$ . This data output follows the data selection table given.
- (i) From this information derive the total expression for the data output. (6 marks)
- (i) Draw the logic diagram for a 4 input multiplexer. (4 marks)
- (b) If the data input for the 4 input multiplexer is given as in Figure Q10 (b), draw the output waveform  $Y$ , in relation to the inputs. (10 marks)
- Q11** (a) (i) Build a full-adder truth table. (3 marks)
- (ii) Using an example of 2 random binary numbers combinations prove your truth table by binary addition method. (2 marks)
- (b) From your truth table in Q11 (a), derive the expression for full adder circuit. (10 marks)
- (c) Draw the circuit for a full adder using the expression derived in Q11 (b) above. (5 marks)

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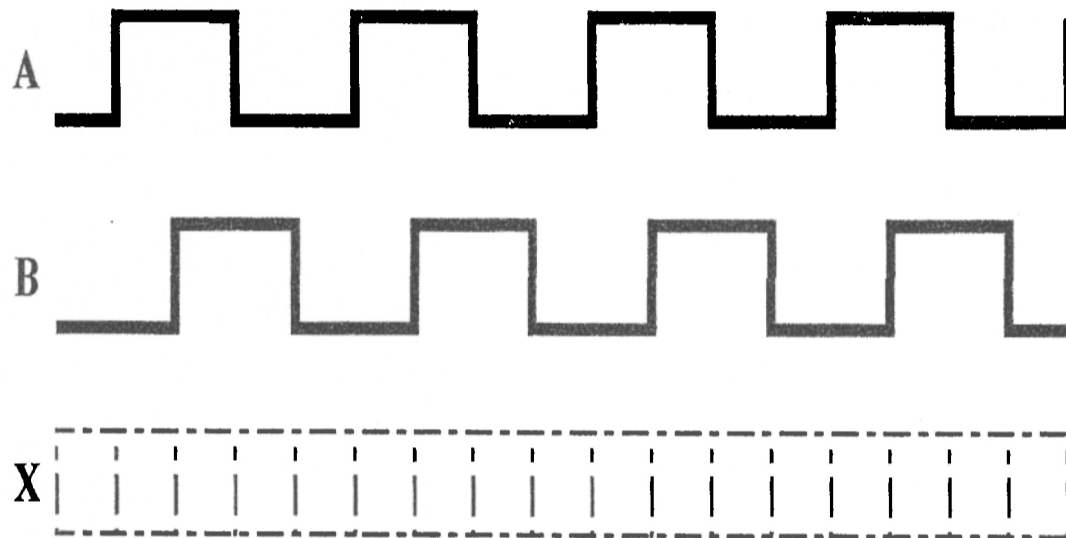


Figure O3 (b). This sheet must be attached with your answer booklet.

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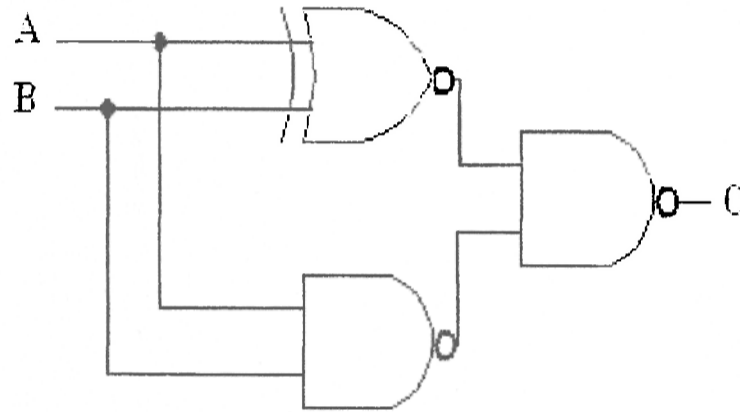
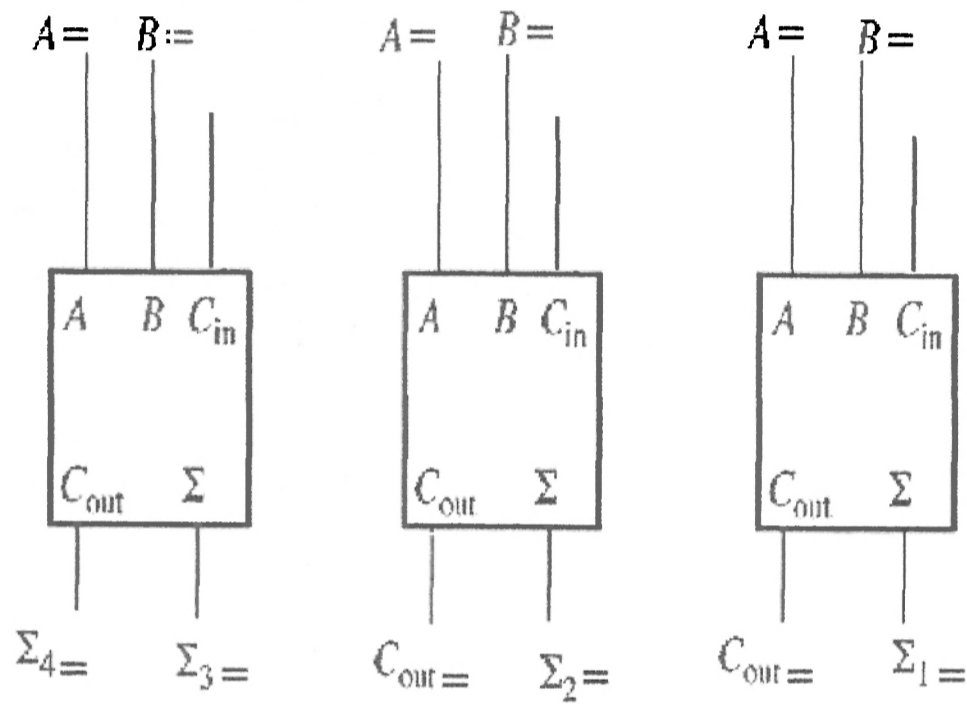


Figure Q4 (c)

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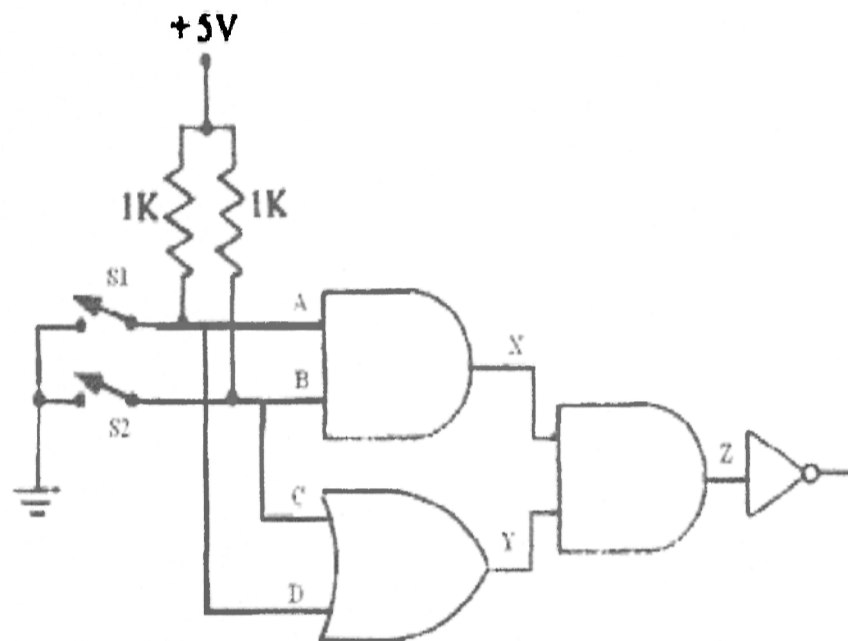
**Figure O6 (b). This sheet must be attached with your answer booklet**



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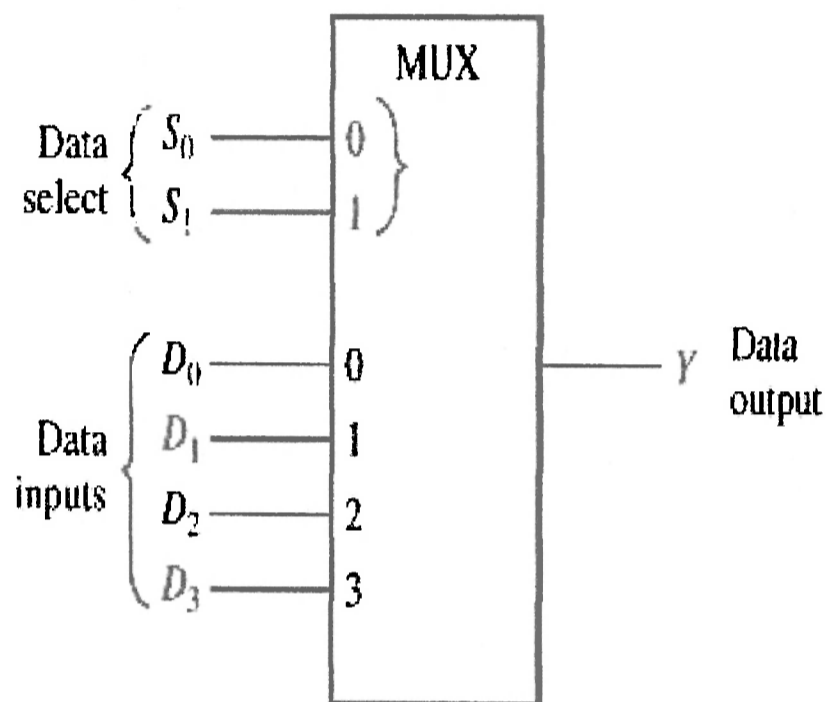
Suis Condition	Input				Output		
	A	B	C	D	X	Y	Z
S1 & S2 Close							
S1 & S2 Open							
S1 Close, S2 Open							
S1 Open, S2 Close							

**Figure Q7. This sheet must be attached with your answer booklet**

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DATA-SELECT INPUTS		INPUT SELECTED
$S_1$	$S_0$	
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

Figure O10 (a)

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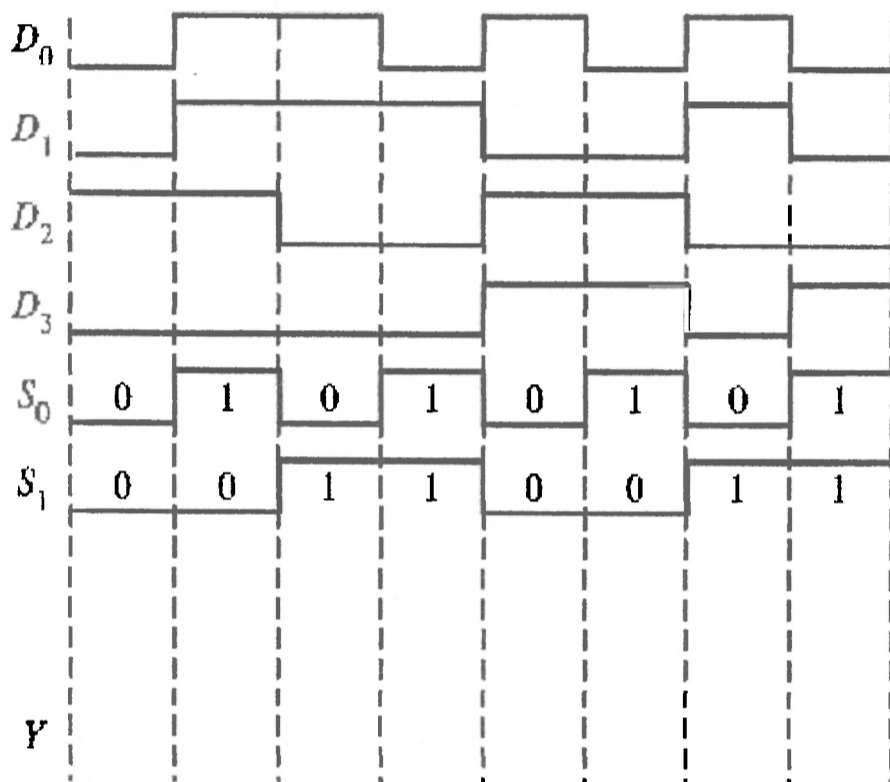


Figure Q10 (b). *This sheet must be attached with your answer booklet.*