UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESION 2008/2009

COURSE NAME	:	DIGITAL SYSTEM DESIGN
COURSE CODE	:	BEE 3133
PROGRAM	:	3 BEE
DATE OF EXAMINATION	:	APRIL/MEI 2009
DURATION	:	2 HOURS 30 MINUTE
INSTRUCTION	:	ANSWER FOUR (4) QUESTIONS ONLY OF SIX (6) QUESTIONS.

THIS QUESTION PAPER CONTAINS EIGHT (8) PAGES

Q1 (a) Predictions of Gordon Moore in 1965 have proved to be remarkably accurate based on transistor growing trends. State the Moore's Laws.

(4 marks)

(b) Transistor becomes smaller, less resistive, faster, conducting more electricity and using less power.

(i) Give a definition of scaling.

(4 marks)

(ii) State THREE (3) goals of technology scaling.

(3 marks)

(iii) Explain briefly THREE (3) types of technology scaling model.

(6 marks)

(iv) Explain briefly FOUR (4) main problems occur in technology scaling and the solution for these problems.

(8 marks)

Q2 (a) VHDL was founded in 1980s by US Department of Defense. It is simply a type of high level computer language used to describe all of the important characteristics of a logic network and also a text based language used to describe hardware.

(i) State THREE (3) types of VHDL modeling.

(3 marks)

(ii) Figure 2(a) illustrates full adder that created using two half adder blocks and an OR gate. Given half_add entity in Figure 2(b), compose VHDL code for the full adder.

(10 marks)

(b) Given logic function $f(x_1, x_2, x_3, x_4) = \sum m(0,1,3,4,7,11,13,15) + D(9,12,14)$.

(i) Synthesize a minimum-cost SOP function.

(6 marks)

(ii) Realize the SOP function using Boolean gates. Assume that the input variables are available in both true and complement.

(4 marks)

(iii) Calculate implementation cost of the SOP function.

(2 marks)

Q3 A sequence detector consists of a single-input and single-output. This sequence detector will produce an output of '1' if the input sequence detects 101 patterns.

(a) Draw a Moore-type state diagram for the sequence detector.

(5 marks)

(b) Derive state table for the detector.

(5 marks)

(c) Derive state-assigned table for the detector.

(2 marks)

(d) Build the detector circuit using D flip-flop.

(5 marks)

(e) Compose VHDL code of the state diagram in Q3(a) using sequential statement.

(8 marks)

Q4 (a) Figure Q4(a) presents a logic circuit constructed using logic gates.
(i) Compute logic expression of the logic circuit.

(3 marks)

(ii) Construct CMOS transistor circuit for the logic circuit.

(10 marks)

(b) Figure Q4(b) shows a stick diagram for a CMOS circuit.
(i) Construct Euler path for the circuit.

(9 marks)

(ii) Write logic equation for the stick diagram.

(3 marks)

Q5 (a) Relate current flow and capacitance charge to small W and large W of a MOSFET.

(6 marks)

(b) For nFET transistor, assume that $k_n' = 100\text{x}10^{-6}\text{A/V}^2$, $W/L = 0.25\mu\text{m}/0.2\mu\text{m}$, $V_{DD} = 5\text{V}$, and $V_{TN} = 1\text{V}$.
(i) Calculate the maximum current flow in the nFET.

(5 marks)

(ii) Determine the aspect ratio needed to obtain a maximum current of 8mA and $W = 5\mu\text{m}$.

(5 marks)

(c) t_{LH} defines as a time needed for the output arise from the $10\%V_{DD}$ to $90\%V_{DD}$ in digital waveform. Given $t_s = \tau_p ln\left(\frac{1}{1-\frac{\cdot}{\cdot\cdot}}\right)$, prove that $t_{LH} = 2.2R_pC_{out}$.

(9 marks)

Q6 (a) Given a simple circuit in Figure Q6(a).

(i) Derive a fault table for the circuit to show the coverage of the various stuck-at-0 and stuck-at-1 faults by the eight possible tests.

(15 marks)

(ii) Find the minimal test set for this circuit.

(4 marks)

(b) Analyze the logic circuit in Figure Q6(b) to identify the tests that can detect each of the faults:

(i) $w_2/0$

(ii) $b/1$

(iii) $d/1$

(6 marks)

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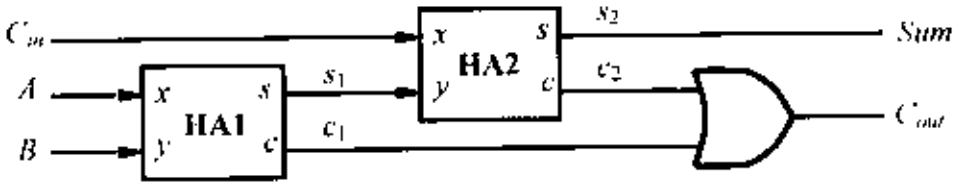

Figure Q2(a)

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY half_add IS
        PORT (x, y : IN     STD_LOGIC;
                s, c : OUT  STD_LOGIC);
END half_add;

ARCHITECTURE LogicFunc OF half_add IS
BEGIN
        s <= x XOR y;
        c <= x AND y;
END LogicFunc ;
```

Figure Q2(b)

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```
PROCESS (w)
        BEGIN
         CASE w IS
                WHEN "1000" =>
                        y <= "11";
                WHEN "0100" =>
                          y <= "10";
                WHEN "0010" ->
                          y <  "01";
                WHEN OTHERS =>
                        y <= "00";
        END CASE;
   END PROCESS;
```

Figure Q3(a)

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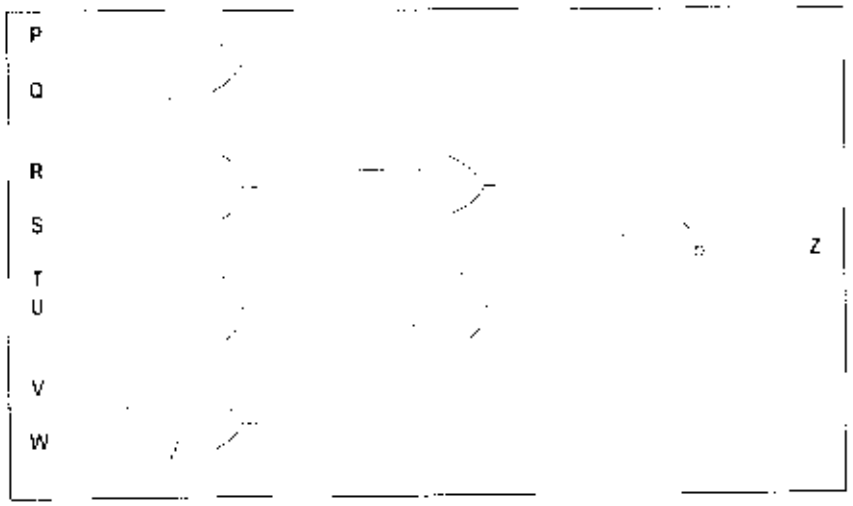

Figure Q4(a)

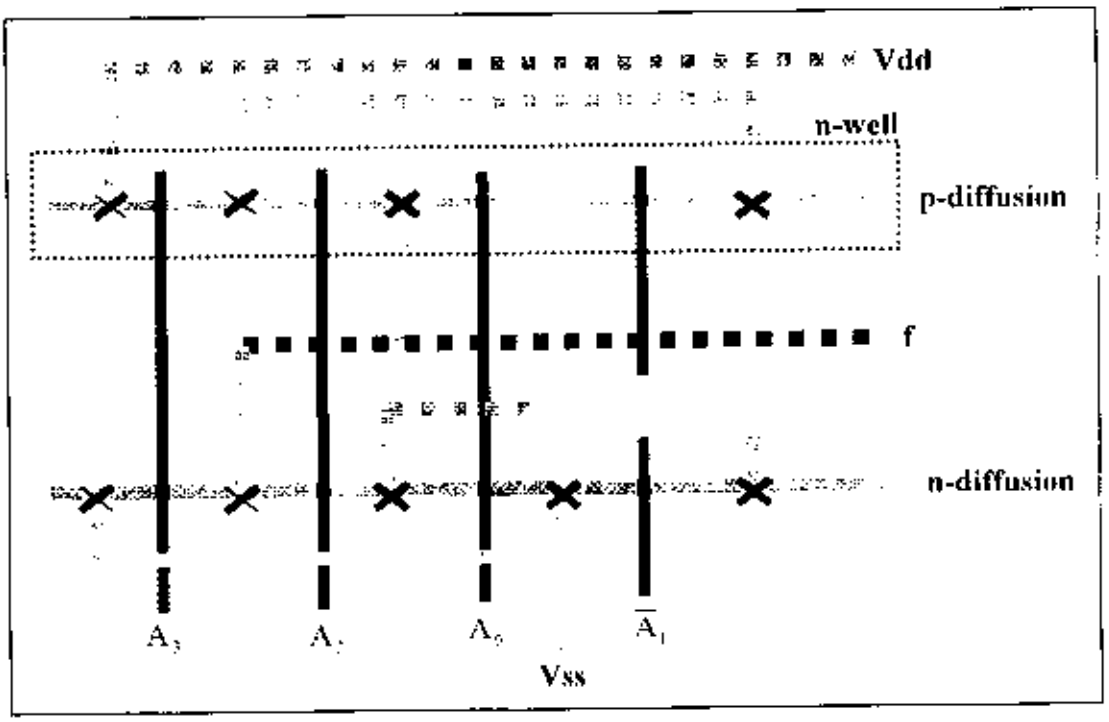

Figure Q4(b)

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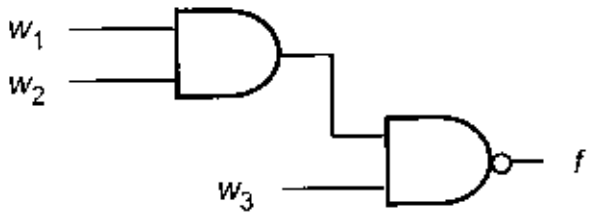

Figure Q6(a)

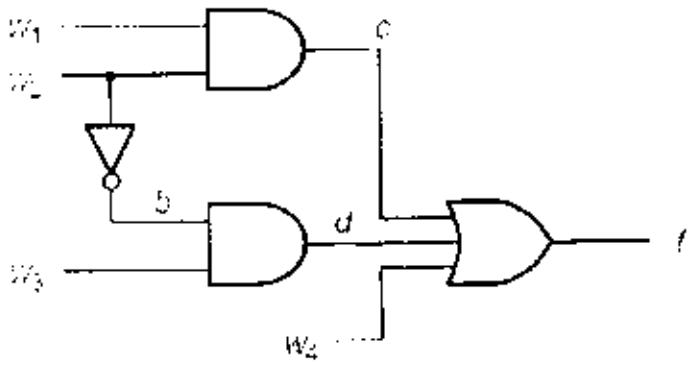

Figure Q6(b)