



KOLEJ UNIVERSITI TEKNOLOGI
TUN HUSSEIN ONN

PEPERIKSAAN AKHIR
SEMESTER I
SESI 2006/07

NAMA MATAPELAJARAN : MIKROPENGAWAL
KOD MATAPELAJARAN : DEK 3133
KURSUS : DET, DEX, DEE
TARIKH PEPERIKSAAN : NOVEMBER 2006
JANGKA MASA : **2 JAM 30 MINIT**
ARAHAN : JAWAB **EMPAT(4)** SOALAN
DARIPADA ENAM(6) SOALAN

KERTAS SOALAN INI MENGANDUNGI 8 MUKA SURAT

SOALAN DALAM BAHASA MELAYU

- S1** (a) Unit Pusat Pemprosesan (CPU) adalah merupakan jantung kepada mikropemproses dimana ia melaksanakan arahan sesuatu program dan juga memproses data. Senaraikan LIMA (5) langkah bagaimana sesuatu program dilaksanakan oleh CPU.
(10 markah)
- (b) Secara ringkasnya sebuah mikropengawal mempunyai semua elemen utama sebuah sistem mikropemproses konvensional dalam satu cip. Nyatakan semua elemen tersebut termasuk rajah strukturnya dan terangkan fungsi setiap elemen.
(15 markah)
- S2** (a) Sampukan adalah satu mekanisma sebuah mikropengawal di mana ia membolehkan ia memberi tindak balas pada satu-satu keadaan pada saat sampukan itu terjadi. Apakah proses yang dipanggil sebagai 'Rutin Layanan Sampukan' (ISR)? Nyatakan EMPAT (4) sumber sampukan.
(10 markah)
- (b) Satu kitar arahan mempunyai empat kitar jam; Q1, Q2, Q3 dan Q4. Apakah yang dipanggil apabila satu arahan dilaksanakan secara efektif dalam satu kitar arahan? Lukiskan satu arahan pelaksanaan berdasarkan pada arahan di bawah dengan tiga kitar arahan.
- ```

 clrw
 movlw 55h
 movwf portb

```
- (15 markah)
- S3** (a) Sebuah mikropengawal menggunakan kristal berkelajuan 1212Hz. Tuliskan aturcara bahasa himpunan untuk lengahan 1 saat.  
(10 markah)
- (b) Berdasarkan litar skematik pada Rajah S3(b), terdapat dua butang masukan (*Clear* dan *Count*) yang disambungkan pada *Port A* (RA0 dan RA1) dan lapan LED disambungkan pada pangkalan B. Butang *Clear* adalah untuk *Reset* (membolehkan memadam pangkalan keluaran) dan Butang *Count* pula adalah untuk pengiraan (membolehkan menokok keluaran). LED akan meningkatkan nilainya apabila butang *Count* ditekan. Tuliskan satu program berdasarkan pada rajah aliran seperti di Rajah S3(b).  
(15 markah)

- S4 (a) Penghimpun langsung adalah arahan yang dimasukkan ke dalam kod sumber PIC di mana ia mengawal operasi penghimpun tersebut. Nyatakan LIMA (5) jenis penghimpun langsung beserta contohnya. (10 markah)
- (b) PIC16F84 mempunyai beberapa ciri-ciri istimewa yang membolehkan dan menambah kelenturan dan julat aplikasi. Ciri-ciri istimewa ini termasuk pengayun. Beri DUA (2) jenis pengayun beserta gambarajah dan nyatakan perbezaan di antara kedua-duanya. (15 markah)
- S5 (a) Rajah S5(a) menunjukkan litar skematik sebuah PIC yang mempunyai satu masukan sampukan pada RB0/INT dan tiga keluaran pada LED (RB1, RB2 dan RB3). Litar beroperasi dengan menyalakan LED secara berjujukan bermula daripada LED1, LED2, LED3, LED1, LED2 dan seterusnya. Lengahan setiap nyalaan adalah selama 1 saat.. Apabila butang SW1 ditekan, sampukan berlaku dimana LED1, LED2 dan LED3 akan berkelip-kelip serentak sebanyak dua kali (4 saat) sebelum kembali semula kepada nyalaan LED mengikut jujukan sebelumnya. Tuliskan aturcara bahasa himpunan untuk PIC melaksanakan operasi tersebut. (25 markah)
- S6 (a) TMR0 adalah daftar fail untuk pemasa larian bebas. Sekiranya jam berkelajuan 4.5 Mhz dibekalkan kepada TMR0 dan dengan tetapan skala 1:256, berapakah masa yang diambil oleh PIC untuk menyelesaikan kiraan 0 sehingga 255? (10 markah)
- (b) (i) 4.5 Mhz frekuensi jam dibekalkan kepada PIC. Berapakah masa yang diambil oleh PIC untuk melaksanakan satu arahan? (10 markah)
- (ii) Berapa arahan yang dapat dilaksanakan oleh PIC tersebut dalam tempoh 2 saat? (5 markah)



**SOALAN DALAM BAHASA INGGERIS**

**Q1** (a) The heart of microprocessor is the Central Processing Unit (CPU) where it executes instructions of the program and process data. List FIVE (5) steps how a program being executed.

(10 marks)

(b) The microprocessor can provide, in a simplified form, all the main elements of the conventional microprocessor system on one chip. List down all the elements including its structure diagram and explain each its function.

(15 marks)

**Q2** (a) Interrupts are a mechanism of a microcontroller which enables it to respond to some events at the moment they occur. What process is called the 'Interrupt Service Routine' (ISR)? List FOUR (4) interrupts sources.

(10 marks)

(b) One instruction cycle has 4 clock cycles; Q1, Q2, Q3 and Q4. What does it called when one instruction is effectively executed in one instruction cycle? Draw an execution instruction based on the program below for three instruction cycle.

```

 clrw
 movlw 55h
 movwf portb

```

(15 marks)

**Q3** (a) The crystal fitted to microcontroller board run at 1212Hz. Write a assembly language program for 1 second delay.

(10 marks)

(b) Based on Figure Q3(b), there are two input buttons (Clear and Count) connected to Port A (RA0 and RA1), and eight LEDs are connected to Port B. Clear button are for Reset (enable to Clear Output Port) while Count Button are for counting (enable to Increment Output). LEDs will increase the value once the Count Button is pressed. Write a program based on the flowchart as shown in Figure Q3(b).

(15 marks)

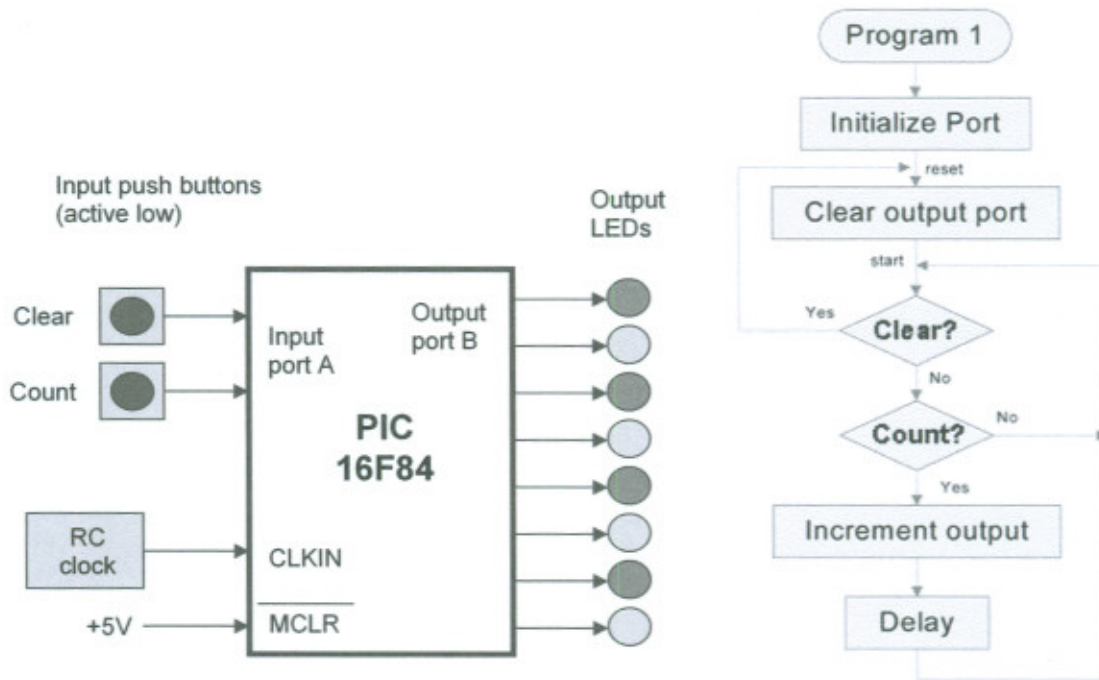
- Q4** (a) Assembler directives are commands inserted in PIC source code which control the operation of the assembler. List FIVE (5) types of directives including examples. (10 marks)
- (b) The PIC16F84 has a number of special features that enhance its flexibility and range of applications. This special feature includes oscillator. Give TWO (2) types of oscillator including diagram and what are the differences between them? (15 marks)
- Q5** (a) Figure Q5(a) shows the schematic circuit of PIC with one interrupt input at RB0/INT and three output LEDs (RB1, RB2 and RB3). The operational of the circuit is to switch ON the LEDs in sequence starting from LED1, LED2, LED3, LED1, LED2 and so on. The delay between every sequence is 1 second. When the SW1 button is pressed, interrupt is activated and at this moment LED1, LED2 and LED3 is blinking simultaneously for two times (4 seconds) before it back to the previous LED pattern instruction sequence. Write an assembly language program for PIC to operate this operation. (25marks)
- Q6** (a) TMR0 is a file register for free run timer. If the 4.5 Mhz clock frequency is feed to TMR0 with the prescaler at 1:256, how long the PIC takes to count from 0 until 255? (10 marks)
- (b) (i) 4.5 Mhz clock frequency is feed to the PIC board. How long PIC need to execute 1 instruction? (10 marks)
- (ii) How many instructions can be execute by the PIC in 2 second? (5 marks)

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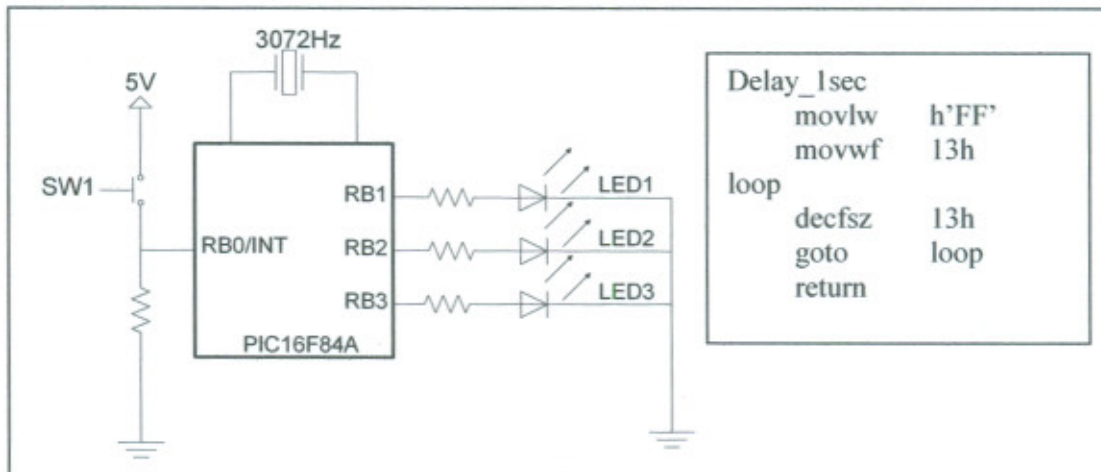
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Senarai Rajah-rajah/ Figures



**Rajah S3(b) / Figure Q3(b)**



**Rajah S5(a) / Figure Q5(a)**



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Jadual 1/Table 1 : Ringkasan Fail-fail daftar khas/ Special Function Register File Summary

| Addr          | Name                  | Bit 7                                                                 | Bit 6  | Bit 5 | Bit 4                                                  | Bit 3           | Bit 2 | Bit 1 | Bit 0     | Value on Power-on RESET | Details on page |
|---------------|-----------------------|-----------------------------------------------------------------------|--------|-------|--------------------------------------------------------|-----------------|-------|-------|-----------|-------------------------|-----------------|
| <b>Bank 0</b> |                       |                                                                       |        |       |                                                        |                 |       |       |           |                         |                 |
| 00h           | INDF                  | Uses contents of FSR to address Data Memory (not a physical register) |        |       |                                                        |                 |       |       |           | ---- ----               | 11              |
| 01h           | TMR0                  | 8-bit Real-Time Clock/Counter                                         |        |       |                                                        |                 |       |       |           | xxxx xxxx               | 20              |
| 02h           | PCL                   | Low Order 8 bits of the Program Counter (PC)                          |        |       |                                                        |                 |       |       |           | 0000 0000               | 11              |
| 03h           | STATUS <sup>(2)</sup> | IRP                                                                   | RP1    | RP0   | $\overline{TO}$                                        | $\overline{PD}$ | Z     | DC    | C         | 0001 1xxxx              | 8               |
| 04h           | FSR                   | Indirect Data Memory Address Pointer 0                                |        |       |                                                        |                 |       |       |           | xxxx xxxx               | 11              |
| 05h           | PORTA <sup>(4)</sup>  | —                                                                     | —      | —     | RA4/T0CKI                                              | RA3             | RA2   | RA1   | RA0       | ---x xxxxx              | 16              |
| 06h           | PORTB <sup>(5)</sup>  | RB7                                                                   | RB6    | RB5   | RB4                                                    | RB3             | RB2   | RB1   | RB0/INT   | xxxx xxxxx              | 18              |
| 07h           | —                     | Unimplemented location, read as '0'                                   |        |       |                                                        |                 |       |       |           | —                       | —               |
| 08h           | EEDATA                | EEPROM Data Register                                                  |        |       |                                                        |                 |       |       |           | xxxx xxxxx              | 13,14           |
| 09h           | EEADR                 | EEPROM Address Register                                               |        |       |                                                        |                 |       |       |           | xxxx xxxxx              | 13,14           |
| 0Ah           | PCLATH                | —                                                                     | —      | —     | Write Buffer for upper 5 bits of the PC <sup>(1)</sup> |                 |       |       | ---0 0000 | 11                      |                 |
| 0Bh           | INTCON                | GIE                                                                   | EEIE   | T0IE  | INTE                                                   | RBIE            | T0IF  | INTF  | RBIF      | 0000 000x               | 10              |
| <b>Bank 1</b> |                       |                                                                       |        |       |                                                        |                 |       |       |           |                         |                 |
| 80h           | INDF                  | Uses Contents of FSR to address Data Memory (not a physical register) |        |       |                                                        |                 |       |       |           | ---- ----               | 11              |
| 81h           | OPTION_REG            | RBPU                                                                  | INTEDG | T0CS  | T0SE                                                   | PSA             | PS2   | PS1   | PS0       | 1111 1111               | 9               |
| 82h           | PCL                   | Low order 8 bits of Program Counter (PC)                              |        |       |                                                        |                 |       |       |           | 0000 0000               | 11              |
| 83h           | STATUS <sup>(2)</sup> | IRP                                                                   | RP1    | RP0   | $\overline{TO}$                                        | $\overline{PD}$ | Z     | DC    | C         | 0001 1xxxx              | 8               |
| 84h           | FSR                   | Indirect data memory address pointer 0                                |        |       |                                                        |                 |       |       |           | xxxx xxxxx              | 11              |
| 85h           | TRISA                 | —                                                                     | —      | —     | PORTA Data Direction Register                          |                 |       |       | ---1 1111 | 16                      |                 |
| 86h           | TRISB                 | PORTB Data Direction Register                                         |        |       |                                                        |                 |       |       |           | 1111 1111               | 18              |
| 87h           | —                     | Unimplemented location, read as '0'                                   |        |       |                                                        |                 |       |       |           | —                       | —               |
| 88h           | EECON1                | —                                                                     | —      | —     | EEIF                                                   | WRERR           | WREN  | WR    | RD        | ---0 x000               | 13              |
| 89h           | EECON2                | EEPROM Control Register 2 (not a physical register)                   |        |       |                                                        |                 |       |       |           | ---- ----               | 14              |
| 0Ah           | PCLATH                | —                                                                     | —      | —     | Write buffer for upper 5 bits of the PC <sup>(1)</sup> |                 |       |       | ---0 0000 | 11                      |                 |
| 0Bh           | INTCON                | GIE                                                                   | EEIE   | T0IE  | INTE                                                   | RBIE            | T0IF  | INTF  | RBIF      | 0000 000x               | 10              |

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.
- 2:** The  $\overline{TO}$  and  $\overline{PD}$  status bits in the STATUS register are not affected by a  $\overline{MCLR}$  Reset.
- 3:** Other (non power-up) RESETS include: external RESET through  $\overline{MCLR}$  and the Watchdog Timer Reset.
- 4:** On any device RESET, these pins are configured as inputs.
- 5:** This is the value that will be in the port output latch.

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Jadual 2/Table 2 : Set-set suruhan/ Instruction Set

| Mnemonic,<br>Operands                         | Description | Cycles                       | 14-Bit Opcode |    |      |      | Status<br>Affected | Notes              |       |
|-----------------------------------------------|-------------|------------------------------|---------------|----|------|------|--------------------|--------------------|-------|
|                                               |             |                              | MSb           |    | LSb  |      |                    |                    |       |
| <b>BYTE-ORIENTED FILE REGISTER OPERATIONS</b> |             |                              |               |    |      |      |                    |                    |       |
| ADDWF                                         | f, d        | Add W and f                  | 1             | 00 | 0111 | dfff | ffff               | C,DC,Z             | 1,2   |
| ANDWF                                         | f, d        | AND W with f                 | 1             | 00 | 0101 | dfff | ffff               | Z                  | 1,2   |
| CLRF                                          | f           | Clear f                      | 1             | 00 | 0001 | 1fff | ffff               | Z                  | 2     |
| CLRWF                                         | -           | Clear W                      | 1             | 00 | 0001 | 0xxx | xxxx               | Z                  |       |
| COMF                                          | f, d        | Complement f                 | 1             | 00 | 1001 | dfff | ffff               | Z                  | 1,2   |
| DECF                                          | f, d        | Decrement f                  | 1             | 00 | 0011 | dfff | ffff               | Z                  | 1,2   |
| DECFSZ                                        | f, d        | Decrement f, Skip if 0       | 1 (2)         | 00 | 1011 | dfff | ffff               |                    | 1,2,3 |
| INCF                                          | f, d        | Increment f                  | 1             | 00 | 1010 | dfff | ffff               | Z                  | 1,2   |
| INCFSZ                                        | f, d        | Increment f, Skip if 0       | 1 (2)         | 00 | 1111 | dfff | ffff               |                    | 1,2,3 |
| IORWF                                         | f, d        | Inclusive OR W with f        | 1             | 00 | 0100 | dfff | ffff               | Z                  | 1,2   |
| MOVF                                          | f, d        | Move f                       | 1             | 00 | 1000 | dfff | ffff               | Z                  | 1,2   |
| MOVWF                                         | f           | Move W to f                  | 1             | 00 | 0000 | 1fff | ffff               |                    |       |
| NOP                                           | -           | No Operation                 | 1             | 00 | 0000 | 0xx0 | 0000               |                    |       |
| RLF                                           | f, d        | Rotate Left f through Carry  | 1             | 00 | 1101 | dfff | ffff               | C                  | 1,2   |
| RRF                                           | f, d        | Rotate Right f through Carry | 1             | 00 | 1100 | dfff | ffff               | C                  | 1,2   |
| SUBWF                                         | f, d        | Subtract W from f            | 1             | 00 | 0010 | dfff | ffff               | C,DC,Z             | 1,2   |
| SWAPF                                         | f, d        | Swap nibbles in f            | 1             | 00 | 1110 | dfff | ffff               |                    | 1,2   |
| XORWF                                         | f, d        | Exclusive OR W with f        | 1             | 00 | 0110 | dfff | ffff               | Z                  | 1,2   |
| <b>BIT-ORIENTED FILE REGISTER OPERATIONS</b>  |             |                              |               |    |      |      |                    |                    |       |
| BCF                                           | f, b        | Bit Clear f                  | 1             | 01 | 00bb | bfff | ffff               |                    | 1,2   |
| BSF                                           | f, b        | Bit Set f                    | 1             | 01 | 01bb | bfff | ffff               |                    | 1,2   |
| BTFSC                                         | f, b        | Bit Test f, Skip if Clear    | 1 (2)         | 01 | 10bb | bfff | ffff               |                    | 3     |
| BTFSS                                         | f, b        | Bit Test f, Skip if Set      | 1 (2)         | 01 | 11bb | bfff | ffff               |                    | 3     |
| <b>LITERAL AND CONTROL OPERATIONS</b>         |             |                              |               |    |      |      |                    |                    |       |
| ADDLW                                         | k           | Add literal and W            | 1             | 11 | 111x | kkkk | kkkk               | C,DC,Z             |       |
| ANDLW                                         | k           | AND literal with W           | 1             | 11 | 1001 | kkkk | kkkk               | Z                  |       |
| CALL                                          | k           | Call subroutine              | 2             | 10 | 0kkk | kkkk | kkkk               |                    |       |
| CLRWDT                                        | -           | Clear Watchdog Timer         | 1             | 00 | 0000 | 0110 | 0100               | $\overline{TO,PD}$ |       |
| GOTO                                          | k           | Go to address                | 2             | 10 | 1kkk | kkkk | kkkk               |                    |       |
| IORLW                                         | k           | Inclusive OR literal with W  | 1             | 11 | 1000 | kkkk | kkkk               | Z                  |       |
| MOVLW                                         | k           | Move literal to W            | 1             | 11 | 00xx | kkkk | kkkk               |                    |       |
| RETFIE                                        | -           | Return from interrupt        | 2             | 00 | 0000 | 0000 | 1001               |                    |       |
| RETLW                                         | k           | Return with literal in W     | 2             | 11 | 01xx | kkkk | kkkk               |                    |       |
| RETURN                                        | -           | Return from Subroutine       | 2             | 00 | 0000 | 0000 | 1000               |                    |       |
| SLEEP                                         | -           | Go into standby mode         | 1             | 00 | 0000 | 0110 | 0011               | $\overline{TO,PD}$ |       |
| SUBLW                                         | k           | Subtract W from literal      | 1             | 11 | 110x | kkkk | kkkk               | C,DC,Z             |       |
| XORLW                                         | k           | Exclusive OR literal with W  | 1             | 11 | 1010 | kkkk | kkkk               | Z                  |       |

- Note** 1: When an I/O register is modified as a function of itself ( e.g., `MOVP PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2: If this instruction is executed on the TMR0 register (and, where applicable,  $d = 1$ ), the prescaler will be cleared if assigned to the Timer0 Module.
- 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.