Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIC 10503
PROGRAMME CODE	:	BIS / BIP/ BIW/ BIM
EXAMINATION DATE	:	DECEMBER 2019/JANUARY 2020
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Show the signed magnitude representation of $+53_{10}$ and -53_{10} in binary representation using 8 bits.

(4 marks)

(b) Convert `1010100001` unsigned binary numbers to decimal.

(1 mark)

(c) Determine `X+Y`, `X-Y` and `X*Y` for the following set of unsigned binary numbers. Show your calculation.

`X= 0011010` `Y= 001100`

(6 marks)

(d) Complete the truth table in **Table Q1(d)** for the following logic circuit in **Figure Q1(d).**

Table Q1(d)

A	B	C	D	M	N	O	P	Q	X	Y	Z
1	0	1	1								
0	1	0	1								
1	1	1	1								
0	1	1	1								
0	1	1	0								
1	0	0	1								
1	0	1	0								

(14 marks)

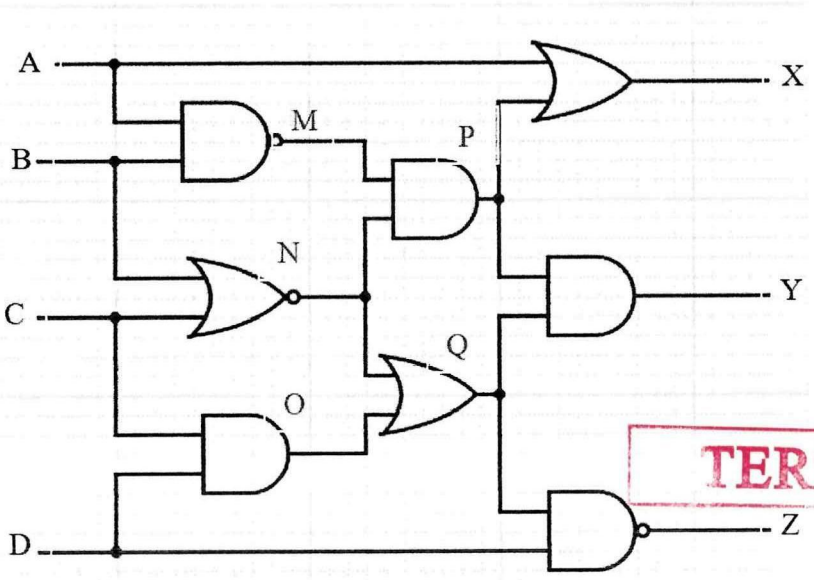

Figure Q1(d)

Q2 (a) List **FIVE (5)** aspects to consider in designing an instruction set.

(5 marks)

(b) **Figure Q2(b)** shows a list of opcodes represented by mnemonics, each with its description.

ADD	Add
SUB	Subtract
MPY	Multiply
DIV	Divide
MOVE	Move data

Figure Q2(b)

Write a machine-language program in symbolic form to compute: `Y = (A - B) / (C + (D x E))` for the following machines.

(i) 2-address machines

(5 marks)

(ii) 3-address machines

(5 marks)

(iii) Based on answers in **Q2(i)** and **Q2(ii)**, analyze the impact of having fewer addresses per instruction.

(4 marks)

(c) Explain **ONE (1)** advantage for each of the following addressing modes.

(i) Immediate Addressing

(2 marks)

(ii) Register Addressing

(2 marks)

(iii) Stack Addressing

(2 marks)

Q3 (a) Discuss **TWO (2)** roles of a register.

(4 marks)

(b) Explain **FIVE (5)** processor tasks to form a complete instruction cycle.

(5 marks)

(c) A processor is designed with a Memory Address Register (MAR), a Memory Buffer Register (MBR), a Program Counter (PC) and an Instruction Register (IR). It is required to run a machine instruction as below.

```
ADD R1, R0, 1
```

Based on the above statement, illustrate and explain the following instruction cycles.

(i) Fetch cycle

(5 marks)

(ii) Indirect cycle

(5 marks)

(d) **Figure Q3(d)** shows the execution of nine instructions in pipeline.

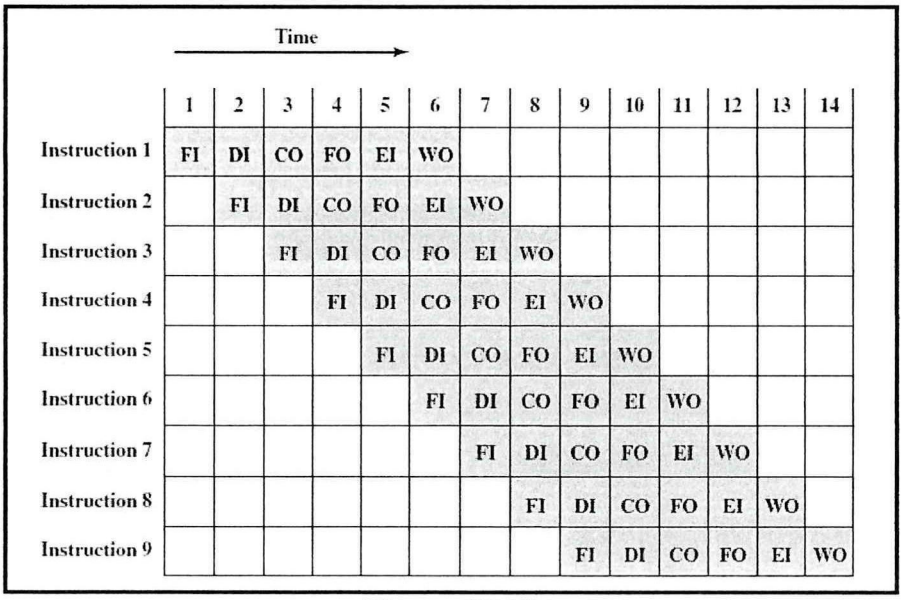

Figure Q3(d)

Illustrate a two-stage pipeline consisting fetch operation and execute operation to run four instructions.

(6 marks)

Q4 (a) Discuss **THREE (3)** steps process which leads to a characterization of a Control Unit.

(3 marks)

(b) **Figure Q4(c)** shows a block diagram of the Control Unit. Explain its **FOUR (4)** inputs and its **TWO (2)** outputs.

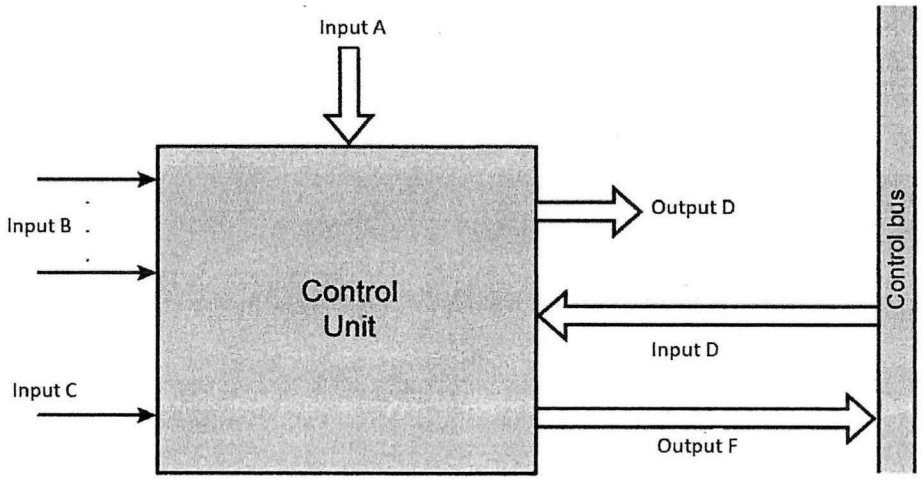

Figure Q4(c)

(12 marks)

- END OF QUESTIONS -