UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2018/2019

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIC 10503
PROGRAMME CODE	:	BIS / BIP/ BIW/ BIM
EXAMINATION DATE	:	JUNE / JULY 2019
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

SECTION A

Instruction: Determine whether each of these statements are TRUE or FALSE.

Q1 Installing extra RAM will speed up your PC.

Q2 USB sticks use ROM so they can store data even after they are removed from the PC.

Q3 An external device attached to the computer by a link to an I/O module. The link is used to exchange control, status, and data between the I/O module and the external device.

Q4 The processor provides signals that control the operation of the ALU and the movement of the data into and out of the ALU.

Q5 A carry-out at the most significant bit after an addition of two signed numbers always indicate overflow. Operation with a negative result will always have carry-out.

Q6 Since the machine-instruction-cycle consists of 4 stages (Fetch-Decode-Execute-Store), 10 instructions require 40 clock cycles.

Q7 Pipelining technique reduce instruction throughput by performing multiple operations in parallel, but does not increases instruction latency.

Q8 The processor updates the Program Counter (PC) after each instruction fetch so that the PC always points to the next instruction to be executed.

Q9 In a bus-organized system, the Memory Address Register (MAR) connects directly to the data bus, and the Memory Buffer Register (MBR) connects to the address bus.

Q10 Multicore processor is known as a chip multiprocessor, combines two or more processor unit on a single piece of silicon.

(10 marks)

SECTION B

Q11 (a) A designer was design two cache memory with same capacity as following specification. The first cache memory organized with larger blocks and the second cache memory organized with small blocks.

Based on above scenario, discuss **ONE (1)** advantage and disadvantage for each memory organization.

(8 marks)

(b) Salpido Sdn Bhd is a multimedia company that provide services of image processing and editing, video editing, video production and live streaming. This company need more space for data storage. The IT Manager was very interested to implement Redundant Array of Independent Disks (RAID) for company storage scheme.
Based on above scenario:

(i) Select the best RAID that suitable for the services provided by the company.

(1 marks)

(ii) Explain **THREE (3)** advantages of your answer in **Q11(b)(i).**

(6 marks)

Q12 (a) Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average 8KB/s on a continuous basis. Determine the percentage of processor time is consumed by this I/O device if it interrupts for every byte. Assume that one interrupt cycle takes 100 µs.

(3 marks)

(b) Based on the Table **Q12(b)**:

TABLE Q12 (b)

Media	File Size	USB 2.0 (480 Mbps)	USB 3.1 (10 Gbps)	USB 3.2 (20 Gbps)
YouTube video	10 MB			
Songs Album	100 MB			
Episode of TV Show	450 MB			
Movie (HD)	10 GB			

(i) Determine the transmission rate for each of media file.

(4 marks)

(ii) Discuss **TWO (2)** key points of the USB's transmission performance from **Q12 (b)(i)**.

(4 marks)

(iii) Discuss the practicality of attaching a USB device directly to a system bus.

(4 marks)

Q13 (a) Show the signed magnitude representation of $+127_{10}$ and -127_{10} in binary representation using 8 bits.

(4 marks)

(b) Compute the sums of the following pairs of unsigned integers. Show your calculation.

(i) `1100 0100 + 0011 0110`

(ii) `0000 1110 + 1010 1010`

(iii) `0111 1111 + 0000 0001`

(6 marks)

(c) Complete the truth table in Table **Q13 (c)** for the following logic circuit in the Figure **Q13 (c).**

(6 marks)

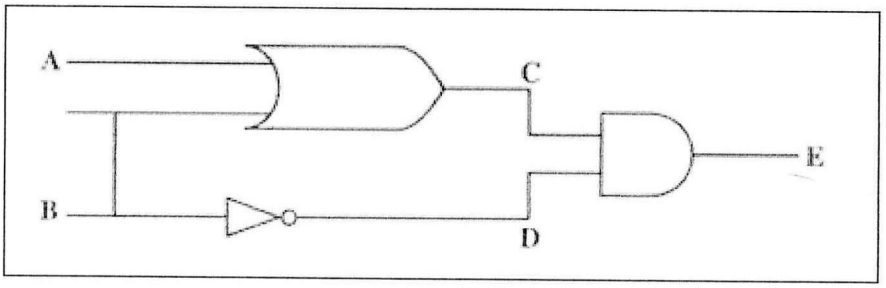

FIGURE Q13 (c)

TABLE Q13 (c)

A	B	C	D	E
0	0			
0	1			
1	0			
1	1			

(d) Complete the truth table in Table **Q13 (d)** for the following logic circuit in the Figure **Q13 (d).**

(4 marks)

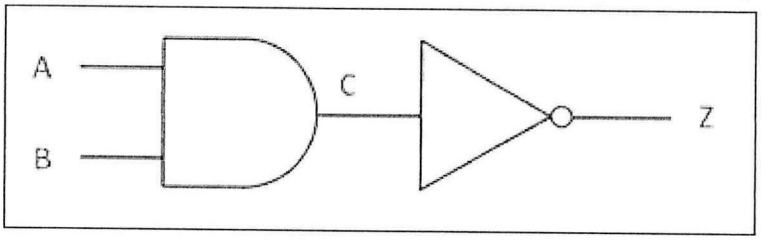

FIGURE Q13 (d)

TABLE Q13 (d)

A	B	C	Z
0	0		
0	1		
1	0		
1	1		

Q14 Trace the execution of the instructions in Table **Q14 (i)** by showing all the changes in CPU registers (control and general purpose registers) as well as the micro-operations. Show the steps and complete the answers in Table **Q14 (ii)**.

(20 marks)

TABLE Q14 (i)

Memory address	Instruction
37C	MOV CX, CHAR
37D	ADD CX, 3
37E	MOV CHAR2, CX

TABLE Q14 (ii)

Clock	PC	MAR	MBR	IR	CX	Micro-operation
t_0						
t_1						
:						
:						

Q15 Table **Q15** shows the micro-operations of fetch cycle, interrupt cycle, and execute cycle of the ADD instruction.
Note: Accumulator (AC), internal registers (Y, Z), Interrupt Service Routine (ISR)

TABLE Q15

Clock cycle	Fetch cycle	Interrupt cycle	Execute cycle of ADD instruction (i.e. ADD AC, X)
T1	MAR ← PC	MBR ← PC	MAR ← X
T2	MBR ← Memory PC ←	MAR ← Save address PC ← ISR	MBR ← Memory
T3	IR ← MBR	Memory ← MBR	Y ← MBR
T4			Z ← AC + Y
T5			AC ← Z

(a) Based on Table **Q15,** give the micro-operations of the execute cycle of the add instruction using the immediate addressing mode (i.e. ADIM AC, X).

(4 marks)

(b) Give the micro-operations of the execute cycle of the add instruction using the indirect mode (i.e. ADIN AC, X).

(6 marks)

Q16 (a) Suggest **ONE (1)** suitable method in designing control unit for a computer that uses Graphics Processing Unit (GPU).

(2 marks)

(b) Give **FOUR (4)** reasons of your suggestion in in **Q16 (a)**.

(8 marks)

- END OF QUESTIONS -