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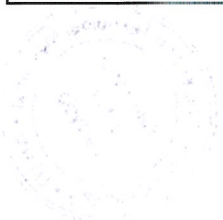
**FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018**

COURSE NAME : COMPUTER ARCHITECTURE
COURSE CODE : BIT 20303
PROGRAMME CODE : BIT
EXAMINATION DATE : JUNE / JULY 2018
DURATION : 3 HOURS
INSTRUCTION : ANSWER ALL QUESTIONS

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THIS QUESTION PAPER CONSISTS OF SIX (6) PAGES

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SECTION A

State either **TRUE (T)** or **FALSE(F)** for each of the following statements.

- Q1** Cache is a small and fast memory. (1 mark)
- Q2** Faster flash drive is needed to overcome the slow operating speed of secondary memory. (1 mark)
- Q3** An interface that provides a method for transferring binary information between internal storage and external devices is called I/O interface. (1 mark)
- Q4** $2^{FAOC_{16}}$ is equivalent to 001011111010 0000 11002. (1 mark)
- Q5** A carry-out at the most significant bit after an addition of two signed numbers always indicate overflow. Operation with a negative result will always have carry-out. (1 mark)
- Q6** Data are exchanged with memory using the Memory Address Register (MAR) and Memory Buffer Register (MBR). (1 mark)
- Q7** Pipelining technique increases instruction throughput by performing multiple operations in parallel, but does not reduce instruction latency. (1 mark)

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Q8 Activating an Arithmetic and Logic Unit (ALU) function is one of the three types of control signal. (1 mark)

Q9 The first step in fetch cycle requires control unit to send a control signal that open gates between MBR and Instruction register (IR) . (1 mark)

Q10 Multi-instance application is an example of effective application for multicore processors. (1 mark)

SECTION B

Q11 Assume that your new laptop running on Windows 10 operating system and equipped with an Intel Core i7-6700HQ. Suggest and explain the amount of suitable RAM size needed based on the **FIVE (5)** activities listed in **Table Q11**. (20 marks)

TABLE Q11

Activities	Amount of suitable RAM (GB) and explanation
Office productivity	
Web browsing	
Media streaming	
Photo editing	
Gaming	

Q12 (a) Illustrate flowcharts of the **THREE (3)** Input/Output (I/O) operation techniques. (6 marks)

(b) Discuss the differences of basic operation for each technique in **Q12(a)**. (9 marks)



Q13 (a) Compute the sum of the following pairs of unsigned integers. Show your calculation.

(i) $1100\ 0100_2 + 0011\ 0110_2$

(ii) $0000\ 1110_2 + 1010\ 1010_2$

(iii) $0111\ 1111_2 + 0000\ 0001_2$

(6 marks)

(b) Compute the following Boolean operations in Table **Q13(b)**.

(14 marks)

TABLE Q13(b)

P	Q	R	$\neg Q$	$P \oplus R$	$Q \wedge R$	$P \vee (Q \wedge R)$	$P \vee Q$	$P \vee R$	$(P \vee Q) \wedge (P \vee R)$
1	1	1							
1	0	0							
1	0	0							
0	1	0							

Q14 (a) (i) Illustrate a pipeline timing diagram of 10 instructions with four stages pipelines: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX).

(4 marks)

(ii) Based on the diagram in **Q14(a)(i)**, state the execution time.

(1 mark)

(b) (i) Draw a data flow diagram of an indirect cycle.

(5 marks)

(ii) Discuss **ONE (1)** difference between indirect and interrupt cycle data flow.

(5 marks)



Q15 (a) Explain in details the sequence of events in fetch cycle as in Figure **Q15(a)**.

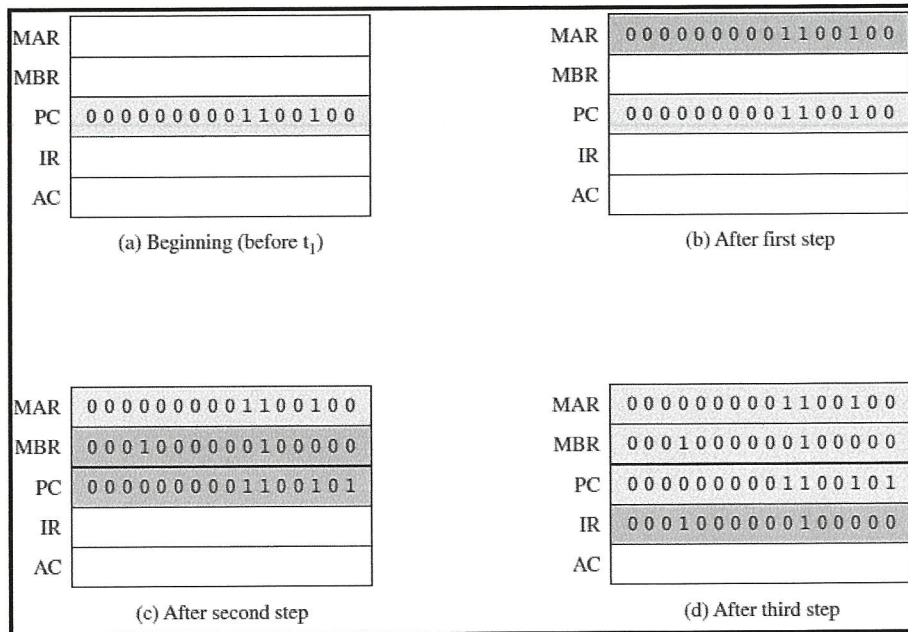


FIGURE Q15(a)

(7 marks)

(b) Rewrite the fetch sequence in Figure **Q15(a)** using symbolic representation.

(3 marks)

Q16 Figure **Q16** shows a general model of the control unit showing all of its inputs and outputs.

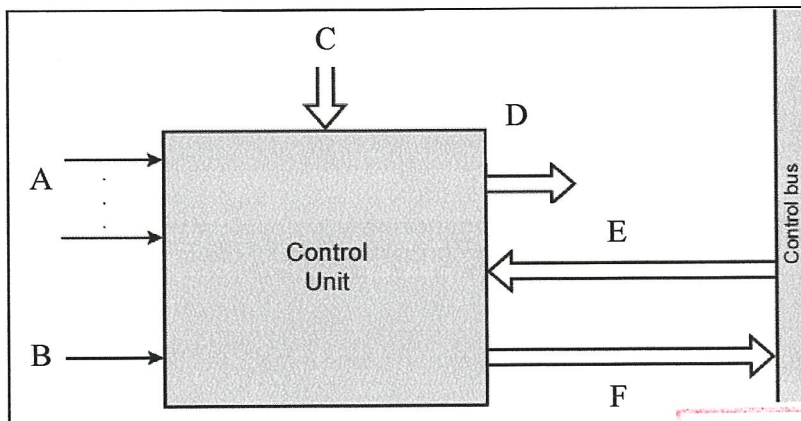


FIGURE Q16

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- (a) Identify **FOUR (4)** inputs of a control unit in Figure **Q16**. (6 marks)

- (b) Explain the flow of inputs and outputs in Figure **Q16**. (4 marks)

- END OF QUESTIONS -

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