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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018**

COURSE NAME : COMPUTER ARCHITECTURE
COURSE CODE : BIC 10503
PROGRAMME CODE : BIS/BIM/BIP/BIW
EXAMINATION DATE : JUNE 2018/ JULY 2018
DURATION : 3 HOURS
INSTRUCTION : ANSWER ALL QUESTIONS

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THIS QUESTION PAPER CONSISTS OF SIX (6) PAGES

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SECTION A**Instruction: Determine whether each of these statements are TRUE or FALSE.**

- Q1** Cache is a small and fast memory. (1 mark)
- Q2** Faster flash drive is needed to overcome the slow operating speed of secondary memory. (1 mark)
- Q3** An interface that provides a method for transferring binary information between internal storage and external devices is called I/O interface. (1 mark)
- Q4** $2FAOC_{16}$ is equivalent to 001011111010 0000 11002. (1 mark)
- Q5** A carry-out at the most significant bit after an addition of two signed numbers always indicate overflow. Operation with a negative result will always have carry-out. (1 mark)
- Q6** Data are exchanged with memory using the Memory Address Register (MAR) and Memory Buffer Register (MBR). (1 mark)
- Q7** Pipelining technique increases instruction throughput by performing multiple operations in parallel, but does not reduce instruction latency. (1 mark)

A red rectangular stamp with the word "TERBUKA" in a bold, serif font, centered within the stamp.

Q8 Activating an Arithmetic and Logic Unit (ALU) function is one of the three types of control signal. (1 mark)

Q9 The first step in fetch cycle requires control unit to send a control signal that opens gates between MBR and Instruction register (IR) . (1 mark)

Q10 Multi-instance application is an example of effective application for multicore processors. (1 mark)

SECTION B

Q11 Random Access Memory (RAM) is the memory that actually lets you work with the data needed to run programs and open files. Whenever your computer loads a program or opens a file, it opens up that data in RAM. If you want to run a program, it pulls the data from long-term storage on your hard drive to short-term storage in RAM, where it can be accessed quickly enough for smooth operation.

The size of RAM needed for a new laptop is depending on user activities. Assume that a new laptop is running on Windows 10 operating system and equipped with an Intel Core i7-6700HQ processor.

Suggest and explain the amount of suitable RAM size needed based on the **FIVE (5)** activities listed in **Table Q11**.

Table Q11

| Activities | Amount of suitable RAM (GB) and explanation |
|------------------------|---|
| i. Office productivity | |
| ii. Web browsing | |
| iii. Media streaming | |
| iv. Photo editing | |
| v. Gaming | |

(20 marks)

Q12 (a) State **THREE (3)** techniques that are possible for I/O operation to read data from a device to memory. (3 marks)

(b) Describe at least **FOUR (4)** major functions of an I/O module. (6 marks)

(c) Describe **THREE (3)** differences between programmed I/O and interrupt I/O. (6 marks)

Q13 (a) Compute the sum of the following pairs of unsigned integers. Show your calculation.

- (i) 1100 0100 + 0011 0110
- (ii) 0000 1110 + 1010 1010
- (iii) 0111 1111 + 0000 0001

(6 marks)

(b) Fill in the blank with correct answer in **Table Q13(b)**.

Table Q13(b)

| P | Q | R | $\neg Q$ | $P \oplus R$ | $Q \wedge R$ | $P \vee (Q \wedge R)$ | $P \vee Q$ | $P \vee R$ | $(P \vee Q) \wedge (P \vee R)$ |
|---|---|---|----------|--------------|--------------|-----------------------|------------|------------|--------------------------------|
| 1 | 1 | 1 | | | | | | | |
| 1 | 0 | 0 | | | | | | | |
| 1 | 0 | 0 | | | | | | | |
| 0 | 1 | 0 | | | | | | | |

(14 marks)



Q14 Trace the execution of the instructions below by showing all the changes in CPU registers (control and general purpose registers) as well as the micro-operations related to the instructions below. Show the steps in a table as shown in **Table Q14**.

| Memory address | Instruction |
|----------------|--------------|
| 39D | MOV CX, NUM |
| 39E | ADD CX, 1 |
| 39F | MOV NUM2, CX |

Table Q14

| Clock | PC | MAR | MBR | IR | CX | Micro-operation |
|----------|----|-----|-----|----|----|-----------------|
| t_0 | | | | | | |
| t_1 | | | | | | |
| : | | | | | | |
| : | | | | | | |
| t_{18} | | | | | | |

(15 marks)

Q15 (a) Explain in details the sequence of events in fetch cycle as in Figure Q15(a).

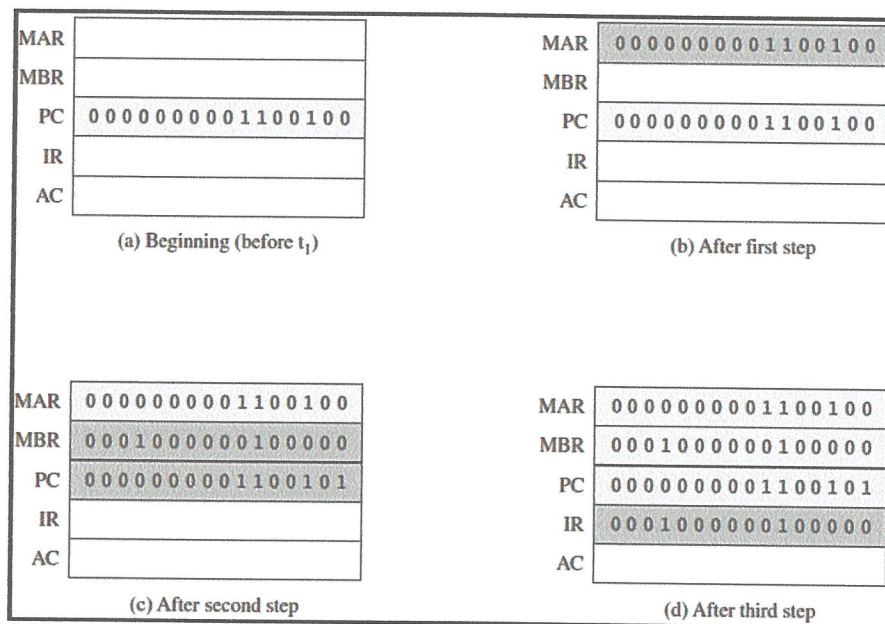


Figure Q15(a)

(7 marks)

(b) Rewrite the fetch sequence in Figure Q15(a) using symbolic representation.

(3 marks)

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Q16 Figure Q16(a) shows a general model of the control unit showing all of its inputs and outputs.

(a) Identify **FOUR (4)** inputs of a control unit in Figure Q16(a).

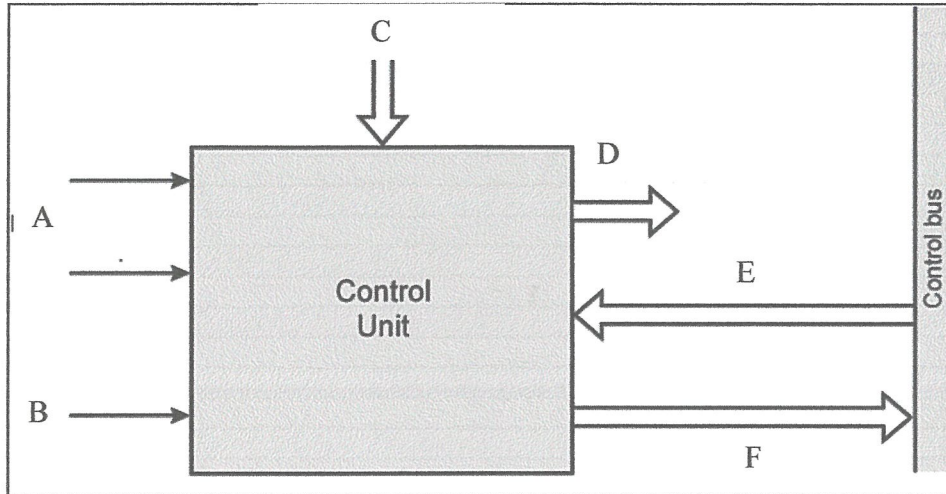


Figure Q16 (a)

(4 marks)

(b) Explain how Control Unit operates.

(6 marks)

- END OF QUESTION -

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