Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	ELECTRONICS
COURSE CODE	:	DAE 21303
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JUNE 2017
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWERS **FOUR (4)** QUESTIONS ONLY

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THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) Briefly explain the difference between conductor, insulator and semiconductor in terms of the number of valence electrons in the valence shell of each material.

(6 marks)

(b) With the aid of an appropriate diagram, describe a PN junction that is:

(i) Forward biased

(4 marks)

(ii) Reversed biased

(4 marks)

(c) Briefly define the following:

(i) Covalent bonding

(2 marks)

(ii) Extrinsic and Intrinsic semiconductor

(2 marks)

(iii) Valence Electron

(2 marks)

(d) (i) Draw and label completely the IV characteristics of a diode which is forward biased.

(3 marks)

(ii) Explain its characteristics.

(2 marks)

Q2 (a) Referring to **Figure Q2(a),** sketch the output waveform by analyzing the circuit operation during its positive and negative cycle. Assume that the diode is in its ideal condition.

(6 marks)

(b) If the circuit in **Figure Q2(a)** is driven by a 60 V_{ac} transformer, with a number of turn ratio of 1:2 and a load resistor of 1.2 kΩ, determine the following by assuming that the diode forward voltage drop is 0.7 V.

(i) Identify the dc load voltage, V_{DC}

(4 marks)

(ii) Indicate the dc current values, I_{DC}

(2 marks)

(iii) Determine the PIV of each diode in the circuit.

(1 marks)

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(c) Given the following circuit as shown in **Figure Q2(c).** By assuming that the diode is an ideal diodes and the f = 1000 Hz, determine Vo for the network shown for the input supply indicated.

(12 marks)

Q3 (a) With the aid of an appropriate diagram, draw with complete labeling, the Common-Emitter circuit configuration for a *npn* bias circuit.

(2 marks)

(b) Sketch the Common-emitter output characteristics with complete determination of the three region of operations.

(3 marks)

(c) For the circuit that has a configuration as shown in **Figure Q3(c),** determine the following values.

(i) Base current, I_B.

(4 marks)

(ii) Collector current, I_C.

(3 marks)

(iii) Collector-Emitter voltage, V_{CE}.

(4 marks)

(iv) Saturation current, $I_{C(SAT)}$.

(3 marks)

(v) Collector-Emitter cut off voltage, $V_{CE(cut\ off)}$

(2 marks)

(vi) Draw a DC load line and plot the Q-point.

(4 marks)

Q4 For the common-emitter amplifier shown in **Figure Q4**, solve the items below.

(a) Compute the ac emitter resistance, r_e'.

(4 marks)

(b) Draw the ac equivalent circuit with complete labeling.

(5 marks)

(c) Calculate the input impedance, Z_i with $r_0 = \infty\ \Omega$

(3 marks)

(d) Indicate the output impedance, Z_0 with $r_0 = \infty\ \Omega$

(3 marks)

(e) Solve the voltage gain, A_V with $r_0 = \infty\ \Omega$

(3 marks)

(f) Recalculate Q5(d) until Q5(e) with $r_0 = 50\ k\Omega$

(4 marks)

(g) Analyze your results in Q5(f).

(3 marks)

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Q5 For the voltage divider biasing circuit shown in **Figure Q5**, determine the following values.

(a) The Q-Point of Drain- current , I_{DQ}

(5 marks)

(b) The Q-Point Of Gate-Source Voltage, V_{GSQ}

(4 marks)

(c) The Drain Voltage, V_D.

(4 marks)

(d) The Source Voltage , V_S

(4 marks)

(e) The Drain- Source Voltage , V_{DS}

(4 marks)

(f) The Drain- Gate Voltage , V_{DG}

(4 marks)

Q6 (a) Briefly explain the purpose of an oscillator and what are the conditions required for a circuit to oscillate.

(5 marks)

(b) By referring to **Figure Q6(b)**, calculate the following ;

(i) Frequency of oscillation.

(3 marks)

(ii) Value of feedback fraction (β).

(3 marks)

(iii) Minimum value of voltage gain (A_V) for the oscillator to start.

(3 marks)

(c) Name the **five (5)** basic elements in a 555 timer IC

(5 marks)

(d) The 555 timer of **Figure Q6(d)** has a value of R_1= 20kΩ , R_2 = 10 kΩ, and C = 0.047 μF.

(i) Calculate the frequency of the output signal

(3 marks)

(ii) Compute the duty cycle

(3 marks)

-END OF QUESTIONS –

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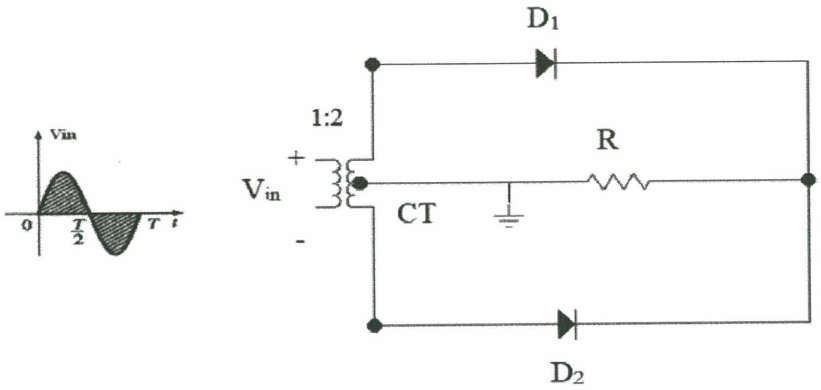

Figure Q2 (a)

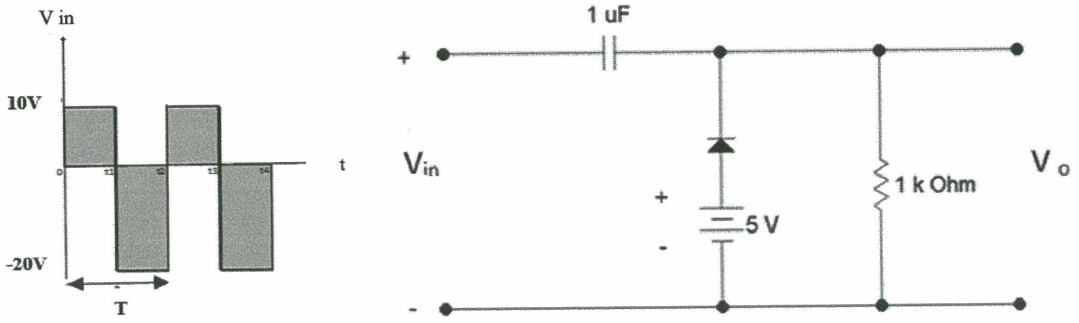

Figure Q2(c)

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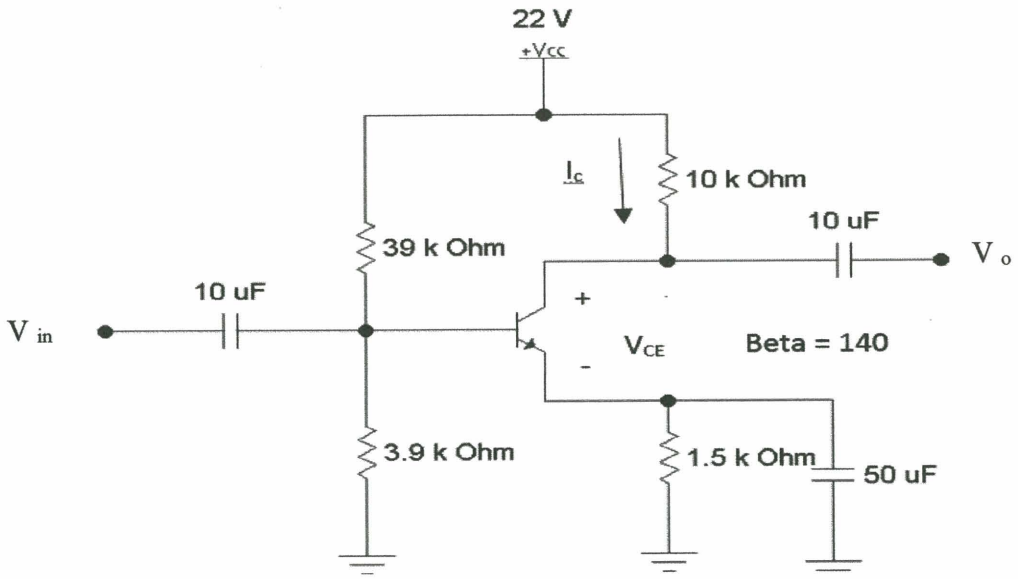

Figure Q3 (c)

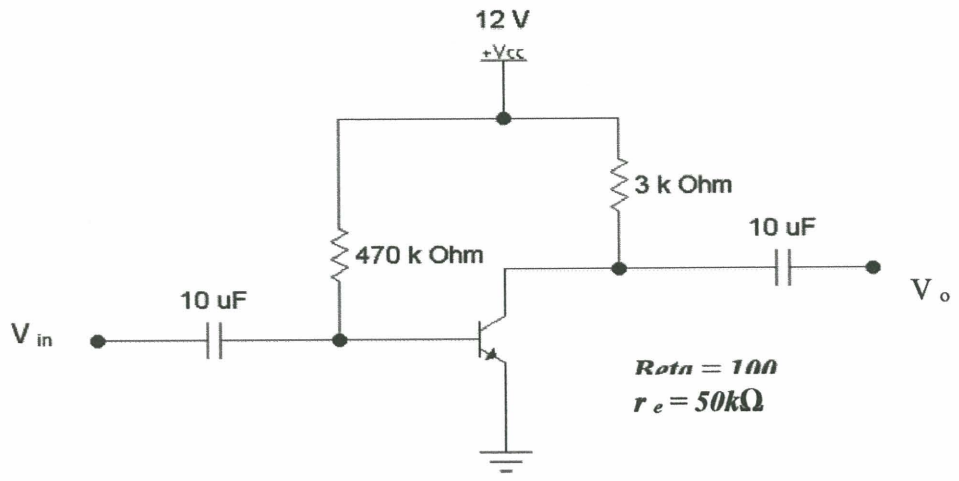

Figure Q4

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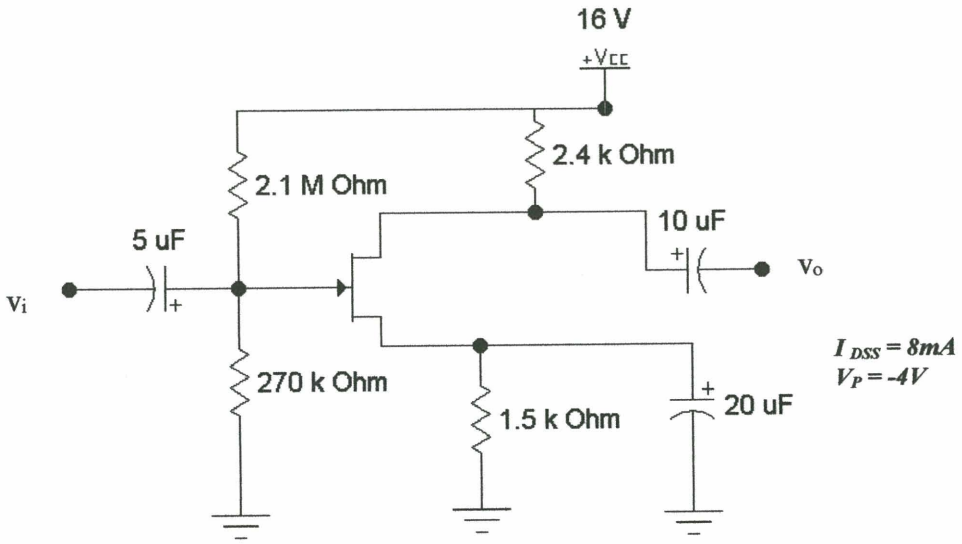

Figure Q5

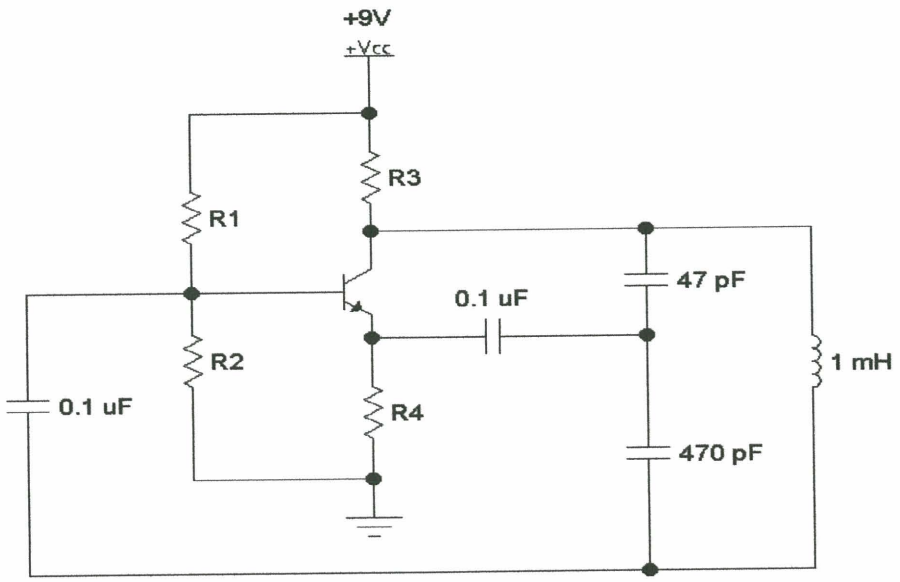

Figure Q6 (b)

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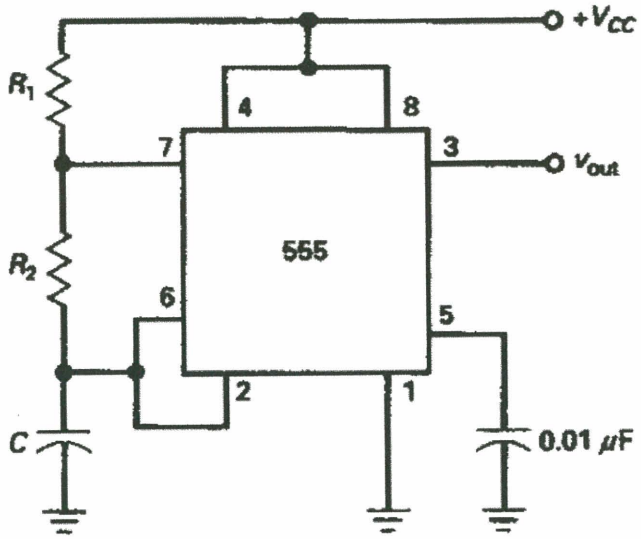

Figure Q6 (d)

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