Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2023/2024

COURSE NAME	:	MICROPROCESSOR AND MICROCONTROLLER
COURSE CODE	:	BEJ 30203
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2024
DURATION	:	3 HOURS
INSTRUCTIONS	:	1. ANSWER ALL QUESTIONS FROM PART A AND ONE QUESTION FROM PART B 2. THIS FINAL EXAMINATION IS CONDUCTED VIA ☐ Open book ☒ Closed book 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

PART A

Q1 Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC) are two different types of microprocessor architecture.

(a) Describe functionality of microprocessor in an electronic system.

(2 marks)

(b) Differentiate RISC and CISC architectures in terms of instruction set, execution time, and complexity of hardware architecture.

(6 marks)

(c) Discuss which microprocessor architecture is suitable for low power implementation in mobile devices. Justify your answer.

(2 marks)

(d) Sketch a basic microprocessor system by showing all bus connections between each component.

(5 marks)

Q2 Digital system typically represents data with size of byte (8-bit), halfword (16-bit) or word (32-bit).

(a) Determine the smallest data size that is suitable to represent the following decimal values.

(i) -128

(1 mark)

(ii) -129

(1 mark)

(iii) 32767

(1 mark)

(b) Given hexadecimal value 0xFFBB is a 2's complement.

(i) Determine the base ten value if the hexadecimal represents halfword value.

(2 marks)

(ii) Determine the base ten value if the hexadecimal represents word value.

(2 marks)

Q3 **Figure Q3.1** illustrates the content of program status register, *xPSR*.

	31	30	29	28	27	26:25	24	23:20	19:16	15:10	9	8	7	6	5	4:0
xPSR	N	Z	C	V	Q	ICI/IT	T			ICI/IT		Exception number				

Figure Q3.1

(a) Determine the value of *N*, *Z*, *V* and *C* flags after a 16-bit microprocessor executes arithmetic operations as follows. Note that the expression is given with decimal radix.

(i) 15088 + 200

(3 marks)

(ii) -2000 + 2000

(3 marks)

(iii) -100 - 200

(3 marks)

(b) Consider the address bus for a 24-bit microprocessor.

(i) Determine the total memory size that can be accessed by the microprocessor.

(2 marks)

(ii) Determine start address and end address of the memory.

(2 marks)

Q4 **Figure Q4.1** shows a disassembly list of an assembly program. Analyse the program and answer the following questions. Note: Refer the datasheet in Appendix A.

1:	0x00000110	480B	LDR	R0, =MyData1
2:	0x00000112	4909	LDR	R1, MyData1
3:	0x00000114	4A09	LDR	R2, MyData2
4:	0x00000116	4B0B	LDR	R3, =0x10000005
5:	0x00000118	F8032C01	STRB	R2, [R3, #-1]
6:	0x0000011C	EA4F2212	LSR	R2, #8
7:	0x00000120	F8032B01	STRB	R2, [R3], #1
8:	0x00000124	EA4F2212	LSR	R2, #8
9:	0x00000128	F8032B01	STRB	R2, [R3], #1
10:	0x0000012C	EA4F2212	LSR	R2, #8
11:	0x00000130	F8032B02	STRB	R2, [R3], #2
12:	0x00000134	7019	STRB	R1, [R3]
13:	0x00000136	BF00	NOP	
14:	0x00000138	MyData1	DCB	"UTHM"
15:	0x0000013E	MyData2	DCD	0x1234ABCD

Figure Q4.1

(a) Determine the content of register R0, R1, R2 and R3 after the instructions at line 1 to 4 have been executed.

(5 marks)

(b) Determine the content of R0, R1, R2 and R3 when program counter, PC contains address 0x00000120.

(4 marks)

(c) Give the size of instruction in Line 8

(2 marks)

(d) Sketch memory from address 0x10000000 to 0x1000000A, then determine the memory content after all instructions have been executed. Assume that these memories initially contain value 0xFF.

(13 marks)

Q5 **Figure Q5.1** shows a simple microcontroller application where two switches and eight LEDs are connected to the microcontroller. The upper four LEDs will turn ON when switch 1 is pressed and the lower four LEDs will turn ON when switch 2 is pressed. All LEDs will be turned ON when both switches are pressed. Based on the specification described, answer the following questions:

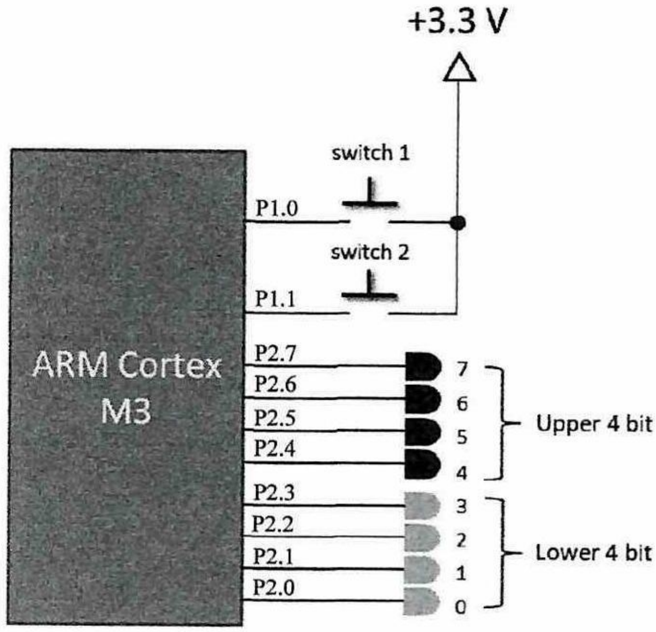

Figure Q5.1

(a) Describe the benefits of using Common Microcontroller Software Interface Standard (CMSIS) to develop ARM-based embedded system.

(2 marks)

(b) Sketch a flowchart to indicate the implementation of the application.

(8 marks)

(c) By using CMSIS, write a C program to implement the application.

(11 marks)

PART B

Q6 Interrupts are important part of the structure of any microprocessor or microcontroller, allowing external events and devices to force a change in CPU activity. Meanwhile, an internal timer is implemented as a hardware peripheral in a microcontroller.

(a) List the most significant actions that a CPU takes when it responds to an enabled interrupt.

(4 marks)

(b) Based on the program in **Figure Q6.1**, write a new program to turn on an LED that is connected to P2.0 whenever the input at P0.0 is changing from 0 to 1 by using interrupt. The LED will remain on if P0.0 remains 1 and will turn off when P0.0 changes to 0.

(8 marks)

```
#include <lpc17xx.h>
void EINT3_IRQHandler(void)
void delay(void);
int main(void)
{
   NVIC_EnableIRQ(EINT3_IRQn);
   LPC_GPIOINT->IO0IntEnF |= (1<<0);
   LPC_GPIO2->FIODIR |= (3<<0);

   while(1)
   {
      LPC_GPIO2->FIOSET |= (1<<1);
      delay();
      LPC_GPIO2->FIOCLR |= (1<<1);
      delay();
   }
}
void EINT3_IRQHandler(void)
{ LPC_GPIO2->FIOPIN ^= (1<<0);
  LPC_GPIOINT->IO0IntClr |= (1<<0);
}
```

Figure Q6.1

(c) A 4.0 MHz clock signal is connected to the inputs of a 12-bit timer. If the timer starts counting from zero, how long does it take before each reaches its maximum value?

(3 marks)

(d) If you are required to design an application that needs precise timings, discuss how a 1 ms timing resolution can be achieved by using the LPC1768 hardware timer. Given the microcontroller is clocked at 100 MHz, the peripheral clock (PCLK) is set at CCLK/4.

(5 marks)

Q7 Serial communication is very useful as it offers a cost-effective way of sending and receiving data. Three communication protocols are often used in microcontroller, i.e. UART, SPI and I2C.

(a) Explain the difference between asynchronous and synchronous serial communication.

(4 marks)

(b) A SPI link is running with a 500 kHz clock. How long does it take for a single message containing one data byte to be transmitted?

(3 marks)

(c) The LPC1768 is configured as I2C master is to be connected to three other LPC1768, each configured as slave. Sketch a circuit showing how this interconnection could be made. Explain your sketch and the advantage of I2C as compared to SPI.

(8 marks)

(d) The timing diagram in **Figure Q7.1** shows the transmission of data packets in an I2C line. Determine the address and data that are transmitted in hexadecimal values.

(5 marks)

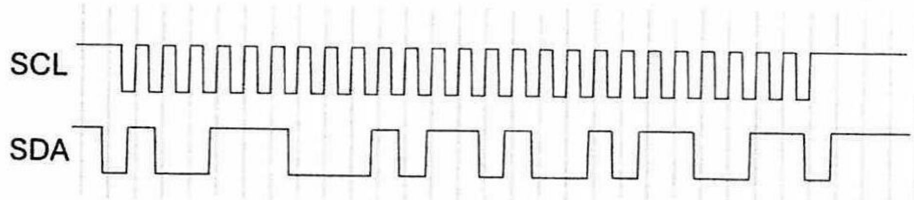

Figure Q7.1

- END OF QUESTIONS -

APPENDIX A

Instruction Set Architecture for Cortex-M3

Mnemonic	Operands	Brief description	Flags
ADD, ADDS	{Rd,} Rn, Op2	Add	N,Z,C,V
ADD, ADDW	{Rd,} Rn, #imm12	Add	N,Z,C,V
AND, ANDS	{Rd,} Rn, Op2	Logical AND	N,Z,C
ASR, ASRS	Rd, Rm, <Rs|#n>	Arithmetic Shift Right	N,Z,C
B	label	Branch	-
BIC, BICS	{Rd,} Rn, Op2	Bit Clear	N,Z,C
BL	label	Branch with Link	-
CMP, CMPS	Rn, Op2	Compare	N,Z,C,V
EOR, EORS	{Rd,} Rn, Op2	Exclusive OR	N,Z,C
LDR	Rt, [Rn, #offset]	Load Register with word	-
LDRB	Rt, [Rn, #offset]	Load Register with byte	-
LDRH	Rt, [Rn, #offset]	Load Register with halfword	-
LSL, LSLS	Rd, Rm, <Rs|#n>	Logical Shift Left	N,Z,C
LSR, LSRS	Rd, Rm, <Rs|#n>	Logical Shift Right	N,Z,C
MOV, MOVS	Rd, Op2	Move	N,Z,C
MOVT	Rd, #imm16	Move Top	-
MOVW, MOV	Rd, #imm16	Move 16-bit constant	N,Z,C
MUL, MULS	{Rd,} Rn, Rm	Multiply, 32-bit result	N,Z
MVN, MVNS	Rd, Op2	Move NOT	N,Z,C
ORN, ORNS	{Rd,} Rn, Op2	Logical OR NOT	N,Z,C
ORR, ORRS	{Rd,} Rn, Op2	Logical OR	N,Z,C
POP	reglist	Pop registers from stack	-
PUSH	reglist	Push registers onto stack	-
ROR, RORS	Rd, Rm, <Rs|#n>	Rotate Right	N,Z,C
RRX, RRXS	Rd, Rm	Rotate Right with Extend	N,Z,C
SDIV	{Rd,} Rn, Rm	Signed Divide	-
SMULL	RdLo, RdHi, Rn, Rm	Signed Multiply (32 x 32), 64-bit result	-
STR	Rt, [Rn, #offset]	Store Register word	-
STRB	Rt, [Rn, #offset]	Store Register byte	-
STRH	Rt, [Rn, #offset]	Store Register halfword	-
SUB, SUBS	{Rd,} Rn, Op2	Subtract	N,Z,C,V
UDIV	{Rd,} Rn, Rm	Unsigned Divide	-
UMULL	RdLo, RdHi, Rn, Rm	Unsigned Multiply (32 x 32), 64-bit result	-

Figure Appendix A