Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2023/2024

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEJ30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2024
DURATION	:	3 HOURS
INSTRUCTIONS	:	1. ANSWER ALL QUESTIONS. PART A NEEDS TO BE ANSWERED IN OMR FORM AND PART B NEEDS TO BE ANSWERED IN THIS BOOKLET. 2. THIS FINAL EXAMINATION IS CONDUCTED VIA ☐ Open book ☒ Closed book 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **TWENTY (20)** PAGES

PART A: OBJECTIVE QUESTIONS (50 MARKS)

Q1 Which register is used to store the value of arithmetic and logical operations?

(a) Accumulator
(b) Address Register
(c) Arithmetic register
(d) Index Register
(e) Data register

(1 mark)

Q2 What is the effective address for ADD R4, 2(PC)

(a) R4 <- R4 + M [PC + 2]
(b) R4 <- R4 + PC + 2
(c) R4 <- M[R4 + PC + 2]
(d) R4 <- M[R4] + M [PC + 2]
(e) R4 <- M[PC + 2]

(1 mark)

Q3 MUL X in one address instruction format means

(a) AC ← AC * X
(b) AC ← AC * M [X]
(c) REG ← AC * M [X]
(d) REG ← REG * X
(e) REG ← REG * M[X]

(1 mark)

Q4 Two main types of branch instructions are _____.

(a) compare and jump
(b) conditional branch and unconditional branch
(c) jump and unconditional branch
(d) logical branch and conditional branch
(e) skip and conditional branch

(1 mark)

Q5 In which mode is the operand placed in one of the general-purpose registers?

(a) Immediate addressing
(b) Implied addressing
(c) Register Indirect
(d) Register mode
(e) Stack pointer mode

(1 mark)

Q6 In the following indexed addressing mode instruction, MOV R1, 2(PC) the effective address is _____.

(a) R1 = R1 + M[PC + 2]
(b) R1 = 2 + M[PC]
(c) R1 = 2 + PC
(d) R1 = 2PC
(e) R1 = M[PC + 2]

(1 mark)

Q7 What is the postfix expression for the following infix expression?

a / b ^ c – d

(a) abc^/d-
(b) ab/cd^-
(c) ab/^cd-
(d) abcd^/-
(e) abcd/^-

(1 mark)

Q8 What is the postfix expression for the corresponding infix expression?

a + b * c + (d * e)

(a) abc+*de*+
(b) abc*+de*+
(c) abc*+(de)*+
(d) ab*c+de+*
(e) a+bc*de+*

(1 mark)

Q9 If a processor clock is rated as 400 billion cycles per second, then its' clock period is:

(a) 2.5×10^{-3}
(b) 2.5×10^{-6}
(c) 2.5×10^{-9}
(d) 2.5×10^{-12}
(e) 2.5×10^{-14}

(1 mark)

Q10 The interrupt-request line is a/an _____, along which the device is allowed to send the interrupt signal.

(a) address line
(b) control line
(c) data line
(d) memory address line
(e) None of the mentioned

(1 mark)

Q11 In memory mapped I/O _____.

(a) a part of the memory is specifically set aside for the I/O operation
(b) the I/O devices and the memory have an associated address space
(c) the I/O devices and the memory share the same address space
(d) the I/O devices have a same address space
(e) the I/O devices have a separate address space

(1 mark)

Q12 The time between the receival of an interrupt and its' services is _____.

(a) cycle time
(b) interrupt delay
(c) interrupt latency
(d) propagation delay
(e) switching time

(1 mark)

Q13 Which of the following are the input devices?

(i) Mouse
(ii) Keyboard
(iii) Monitor
(iv) Microphone

(a) i, ii, and iii
(b) i, ii, and iv
(c) i, iii, and iv
(d) ii, iii, and iv
(e) i, ii, iii and iv

(1 mark)

Q14 Why is the device synchronization process needed?

(a) to increase the device's versatility
(b) to balance up the transfer rate between I/O device and the processor
(c) so the bandwidth of the device can reach the maximum limit of transfer rate
(d) to reduce the cost
(e) so that the device can easily be added

(1 mark)

Q15 An interrupt that are caused by software are called

(a) exception interrupts
(b) special interrupts
(c) normal interrupt
(d) hardware interrupts
(e) controlled interrupts

(1 mark)

Q16 The system is notified of a read or write operation by _____

(a) appending an extra bit of the addres
(b) enabling the read or write bits of the devices
(c) sending a special signal along the BUS
(d) raising an appropriate interrupt signal
(e) handshake signal handling

(1 mark)

Q17 How can the processor ignore other interrupts when it is servicing one?

(i) By disabling the devices from sending the interrupts.
(ii) By increasing the number of program counter
(iii) By turning off the interrupt request line.
(iv) By using edge-triggered request line

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q18 Input and output devices are notified of a read or write operation by _____.

(a) enabling the read or write bits of the devices
(b) pending an extra bit of the address
(c) raising an appropriate interrupt signal
(d) sending a special signal along the BUS
(e) sending a read or write bits of the devices

(1 mark)

Q19 The method which offers higher speeds of I/O transfer is _____.

(a) interrupt
(b) memory mapping
(c) Program-controlled I/O
(d) Direct Memory Access (DMA)
(e) I/O mapped I/O

(1 mark)

Q20 Which register holds instructions/data temporarily after it is brought to the processor from main memory?

(a) General Purpose Register
(b) Instruction Register
(c) Memory Address Register
(d) Memory Data Register
(e) Program Counter

(1 mark)

Q21 What happens immediately after data is returned to the Memory Data Register (MDR) from memory in the Fetch stage?

(a) Data from the MDR is copied into the Memory Address Register
(b) Data from the MDR is copied into the Instruction Register
(c) Data from the MDR is copied into the Program Counter
(d) Data from the MDR is sent back to memory along the data bus
(e) Data from the MDR is sent to address register

(1 mark)

Q22 CPU performance can be affected by:

(i) Cache size
(ii) Clock speed
(iii) Number of cores
(iv) Number of instructions in a program

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q23 Which of these happen in the Fetch stage?

(i) the Program Counter is incremented by one
(ii) the value in the Program Counter is sent to memory on the address bus
(iii) the value returned from memory is added to the value in the Memory Address Register
(iv) the value returned from memory is stored in the current instruction register

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q24 Which of the following happen in the Execute stage?

(i) Data from memory is copied into the Accumulator
(ii) Data from memory and Accumulator are executed
(iii) The Program Counter value is copied into the Memory Address Register
(iv) Data from memory is added to the Accumulator, and the result is stored there

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q25 Which of the following does not happen in the Execute stage?

(i) The ALU executes the instruction for the value in the Accumulator
(ii) The control unit decodes the IR to determine the data value
(iii) The data in the IR is added to the value in the Memory Data Register
(iv) The data in the IR is copied into the Memory Address Register

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q26 LOAD X means:

(a) Load the current Memory Address Register value to address X
(b) Load the current Memory Data Register value with address value of X
(c) Load the value in Memory Address Register with address value of X to the accumulator
(d) Load the X value to Memory Address Register
(e) Load the X value to Memory Data Register

(1 mark)

Q27 _____ show one of the processes happen in Fetch stage.

(a) AC ← MDR + [AC]
(b) IR ← PC
(c) MAR ← PC
(d) MDR ← PC
(e) PC ← [PC] + Branch offset

(1 mark)

Q28 Cache memory acts between _____.

(i) CPU
(ii) RAM
(iii) External Hard Disk
(iv) Secondary Storage

(a) i and ii
(b) i and iii
(c) ii and iii
(d) ii and iv
(e) iii and iv

(1 mark)

Q29 How many bytes does a memory can be contained if it has 1500 words of 256 bits each?

(a) 384 Kbyte
(b) 384000 Kbyte
(c) 48 Kbyte
(d) 4800 Kbyte
(e) 48000 Kbyte

(1 mark)

Q30 The purposes of ROM are _____

(i) booting purposes
(ii) arithmetic execution purposes
(iii) store the permanent information
(iv) they do not lose memory when power is removed

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q31 Which statement best describes ROM?

(a) A flash memory chip that contains a small amount of non-volatile memory
(b) A memory store containing a large amount of volatile memory
(c) A memory store containing a small amount of volatile memory
(d) A memory which used to store data on a temporary basis
(e) A register within the CPU responsible for storing memory addresses

(1 mark)

Q32 In comparison with static RAM memory, the dynamic RAM memory is _____.

(i) higher in bit density
(ii) faster
(iii) expensive
(iv) cheaper

(a) i and iii
(b) i and iv
(c) ii and iii
(d) ii and iv
(e) None of the mentioned

(1 mark)

Q33 How many 128kB RAM chips are needed to provide a memory capacity of 16384kB?

(a) 64
(b) 128
(c) 256
(d) 512
(e) 1024

(1 mark)

Q34 If a memory has 50 cache hits and 30 misses, the cache miss rate is _____.

(a) 37.5%
(b) 60.0%
(c) 62.5%
(d) 66.6%
(e) 80.0%

(1 mark)

Q35 When is Virtual Memory needed or used by a computer?

(i) When chosen by the user or computer administrator
(ii) When multitasking is required
(iii) When RAM becomes full because of too many programs running at once
(iv) When users wish to store data on an external server such as cloud server
(v) When users wish to use large programs

(a) i, ii and iii
(b) i, ii, and iv
(c) ii, iii and iv
(d) ii, iii, and v
(e) iii, iv, and v

(1 mark)

Q36 Which of the following statements are not correct about the main memory of a computer?

i) In main memory, data gets lost when power is switched off
ii) Main memory including both RAM and ROM
iii) Main memory is faster than registers
iv) Main memory is smaller than cache

(a) i, ii and iii
(b) i, ii and iv
(c) i, iii, and iv
(d) ii, iii and iv
(e) i, ii, iii, and iv

(1 mark)

Q37 A non-pipeline system takes 50ns to process an instruction. The same instruction can be processed in five-segment pipeline with a clock cycle of 10ns for each segment. By considering that there is no hazard happen in the system, determine approximately the speedup ratio of the pipeline for 500 instruction.

(a) 4
(b) 4.5
(c) 4.96
(d) 5
(e) 5.30

(1 mark)

Q38 Which of the following are advantages of pipelining?

(i) Faster ALU can be designed when pipelining is used
(ii) Increase in the number of pipeline stages increases the number of instructions executed simultaneously.
(iii) Instruction latency increases in pipelined processors.
(iv) Pipelining increases the overall performance of the CPU

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q39 Hazard in pipeline including _____.

(i) data hazard
(ii) execution hazard
(iii) instruction hazard
(iv) structural hazard

(a) i, ii and iii
(b) i, ii, and iv
(c) i, iii and iv
(d) ii, iii, and iv
(e) i, ii, iii, and iv

(1 mark)

Q40 To increase the speed of memory access in pipelining, we make use of _____.

(a) buffers
(b) cache
(c) random access memory
(d) special memory locations
(e) special purpose registers

(1 mark)

Q41 The following is TRUE about the Cache features except

(a) It is expensive
(b) It stores the frequently used data and instruction
(c) Cache hit will increase the processor time
(d) The cache storage is bigger than general purpose register storage size
(e) The cache storage will decrease the latency time

(1 mark)

Q42 Which of the following is disadvantage of pipelining?

(a) The cycle time of the processor is reduced
(b) Increase the CPU performance
(c) Increase the required memory
(d) The design of pipelined processor is costly to manufacture
(e) The instruction latency is less

(1 mark)

Q43 If a unit completes its task before the allotted time period, then _____.

(a) it will perform some other task in the remaining time
(b) it gets reallocated to a different task
(c) it will reduce the allotted time period
(d) it remains idle for the remaining time
(e) none of the mentioned

(1 mark)

Q44 The conflict for the usage of a hardware device is called _____.

(a) Hardware hazard
(b) Pipeline hazard
(c) Data hazard
(d) Instruction hazard
(e) Structural hazard

(1 mark)

Q45 The period of time when the unit is idle is called as_____.

(a) stalls
(b) bubbles
(c) stalk
(d) deadlock
(e) both stalls and bubbles

(1 mark)

Q46 Which of the following is/are correct statement/statements about Cloud Computing?

(a) Cloud Computing does not have any impact on software licensing
(b) Cloud Computing does not suffer from latency connectivity
(c) Cloud Computing presents new opportunities to users and developers
(d) Cloud Computer is nothing more than the Internet
(e) All of the mentioned

(1 mark)

Q47 Which statement is not true about a cloud computing environment?

(i) It is invulnerable to data loss
(ii) It enables users to access systems regardless of their location
(iii) It introduces latency as the servers are geographically dispersed
(iv) It can increase the capital expenses for hardware and software setting up

(a) i, ii, and iii
(b) i, ii, and iv
(c) i, iii, and iv
(d) ii, iii, and iv
(e) None of the mentioned

(1 mark)

Q48 What are some of the cloud benefits that make it a lower risk for enterprises to adopt the cloud?

(i) Data security associated with loss or unavailability of data causing business disruption
(ii) Diversity of standards for technology integration leads to data leakage
(iii) The pay-as-you-go model allows enterprises to experiment with technologies as opposed to making long-term decisions based on little or no trial
(iv) The speed with which applications can be up and running on the cloud versus months on traditional platforms, means enterprises can experiment, fail fast, learn, and course correct without setting them back significantly

(a) i and ii
(b) i and iv
(c) ii and iii
(d) ii and iv
(e) iii and iv

(1 mark)

Q49 Which of the following is/are the application of cloud computing?

(a) Adobe
(b) Paypal
(c) Netflix
(d) Google G Suite
(e) All of the mentioned

(1 mark)

Q50 A company that originally planned its web-based IT system to support 10,000 users suddenly notices that there is four times increase in demand. If the company has deployed its system in a true cloud environment, what are the incremental maintenance costs to adding new resources to this environment?

(a) Twice its original costs of deployment
(b) Three times its original costs of deployment
(c) Four times its original costs of deployment
(d) Eight times its original costs of deployment
(e) Small or no cost at all

(1 mark)

PART B: SUBJECTIVE QUESTIONS (50 MARKS)

Q51 Memory is used to store data or instructions needed for task execution. Explain the differences between:

(a) Primary and Secondary storage in terms of accessibility to processor.

(2 marks)

(b) Cache Hit and Cache Miss.

(2 marks)

Q52 Consider an equation is executed using CISC one address format and it is illustrated in memory address as **Figure Q52.1**:

MAR	MDR
100	LOAD 110
101	SUB 113
102	DIV 112
103	STORE 110
104	LOAD 114
105	MUL 111
106	ADD 110
107	STORE 114
108	
109	
110	55
111	2
112	7
113	20
114	5

Figure Q52.1 : Value in Memory before executing the CISC instructions

Calculate the final value of Memory Data Register (MDR) for Memory Address Register (MAR) 110 till 114 after the CISC instruction in MAR 100 till 107 is executed. Write your answer in **Figure Q52.2.**

MAR	MDR
110	
111	
112	
113	
114	

Figure Q52.2: Value in Memory after executing the CISC instructions

(5 marks)

Q53 Assume that an opcode is in **Table Q53.1** and content in the Memory Address Register (MAR) is in **Figure Q53.1**.

Table Q53.1: List of Opcode

0000 = Halt
0001 = Load AC from Memory
0010 = Store AC to Memory
0011 = Multiply to AC from Memory
0100 = Subtract to AC from Memory
0101 = Add to AC from Memory

The initial values for Memory, Program Counter (PC), Accumulator (AC), and Instruction Register (IR) are as in **Figure Q53.1**.

MAR	MDR
410	0889
411	1886
412	4885
413	3887
414	5889
415	2888
...	
...	
885	0008
886	0030
887	0002
888	0074
889	0006

CPU Register

PC	411
AC	0
IR	0

Figure Q53.1: The initial value for Memory, Program Counter (PC), Accumulator (AC) and Instruction Register (IR)

(a) Calculate the final value of PC, AC and IR after executing instructions till MAR 415.

(6 marks)

PC	
AC	
IR	

(b) Calculate the new value stored in M[888].

(2 marks)

Q54 Consider a system with multiple-level memory with parameters as shown in **Figure Q54.1**.

Memory	Hit time	Miss Rate
L1-cache	0.5 ns	20%
L2-cache	1.8 ns	5%
L3-cache	4.2 ns	1.5%
Main Memory	70 ns	0%

Figure Q54.1: A system with multiple-level memory

Calculate Average Memory Access Time (AMAT) for the whole system.

(9 marks)

Q55 Pipelining is a technique for improving the performance of a CPU by breaking down instructions into smaller steps and executing them simultaneously in different hardware units. This allows the CPU to start working on the next instruction before the previous instruction has finished executing. CPU X has a set of instructions to run, as shown in **Listing Q55.1**. The instruction format for instructions in **Listing Q55.1** is shown in **Figure Q55.1**.

```
MOV R1, #3
MOV R2, #4
MUL R1, R2
MOV R3, R1
```

Listing Q55.1: Set of instructions to run

Operation	Destination Operand	Source operand

Figure Q55.1: The instruction format

The execution of each instruction involves five steps, including Fetch Instruction, Decode, Read Operand, Execute and Write Result.

Assume that this pipeline system uses:
One cycle to perform Fetch Instruction (FI),
One cycle to perform Decode (D),
Two cycles to Read Operand (RO),
Two cycles to perform Execution (E),
One cycle to perform Write Result (WR).

(a) Produce the final value in register R3 at the end of **Listing Q55.1** instructions.

(1 mark)

(b) Illustrate the space time diagram to execute the instructions in **Listing Q55.1** using non-pipelined method.

(3 marks)

(c) Illustrate the space time diagram to execute the instructions in **Listing Q55.1** using pipeline method.

(3 marks)

(d) Compare the Cycle per Instruction (CPI) for both non-pipelined and pipeline methods. Calculate the speedup factor for these systems.

(2 marks)

Q56 Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. **Table Q56.1** shows the measurements recorded on the two machines running a given set of benchmark programs:

Table Q56.1

Instruction Type	Instruction Count	Cycles per Instruction
Machine A		
Arithmetic Operation	8 000 000	1
Data Transfer	4 000 000	3
Floating Point	2 000 000	4
Control Operation	4 000 000	3
Machine B		
Arithmetic Operation	10 000 000	1
Data Transfer	8 000 000	2
Floating Point	2 000 000	4
Control Operation	4 000 000	3

Calculate:

(a) Cycle per Instruction (CPI) for both Machine A and Machine B.

(4 marks)

(b) Million Instruction per Second (MIPS) for both Machine A and Machine B.

(4 marks)

(c) Execution time for both Machine A and Machine B.

(4 marks)

Q57 Cloud computing is an on-demand availability of computer resources especially on cloud database and power computing.

(a) Identify **TWO (2)** Cloud database that are commonly used by the user.

(1 mark)

(b) There are multiple benefit when it deal with cloud computing. Explain **TWO (2)** cloud computing benefit to small scale business.

(2 marks)

- **END OF QUESTIONS –**