Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2023/2024

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEJ 10603 / BEV 10603
PROGRAMME CODE	:	BEJ / BEV
EXAMINATION DATE	:	JULY 2024
DURATION	:	3 HOURS
INSTRUCTIONS	:	1. ANSWER ALL QUESTIONS 2. THIS FINAL EXAMINATION IS CONDUCTED VIA ☐ Open book ☒ Closed book 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES.

Q1 (a) **Figure Q1.1** shows four switches that are part of a control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open and as the paper passes over a switch, the switch closes. Design and draw the logic circuit to produce a HIGH output whenever three or more switches are closed at the same time. Use Karnaugh mapping to solve this problem. In your design, assume that SW1 is the Most significant bit (MSB) and SW4 is the Least significant bit (LSB). Note that the switch will be LOW when it closes.

(10 marks)

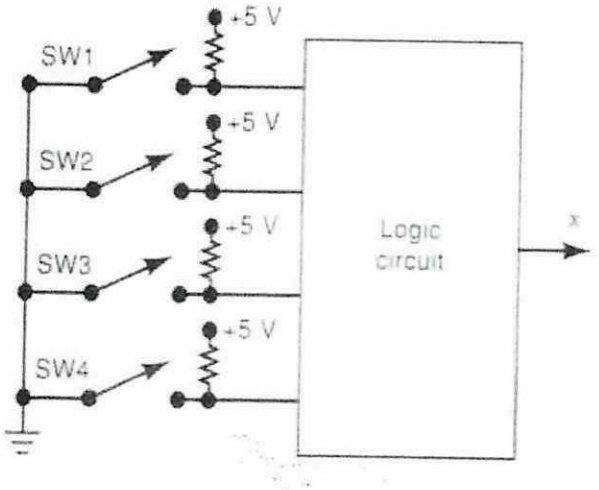

Figure Q1.1

(b) Simplify the Boolean expression using Karnaugh map. Draw the simplified logic circuit.

$$f(w,x,y,z)=\sum m\,(0,3,5,7,8,9,10,12,13) + \sum d\,(1,6,11,14)$$

(6 marks)

(c) A 3-bit binary number is represented by A B C with A is the MSB and C is the LSB. Construct a combinational logic circuit, which produce an output HIGH when the binary number A B C are more than 3_{10} and less than 7_{10}. Use truth table and Karnaugh Map in your answer. Show all steps.

(9 marks)

Q2 (a) **Figure Q2.1** shows a multiplexer 74LS151 (8 line-to-1 line multiplexer).

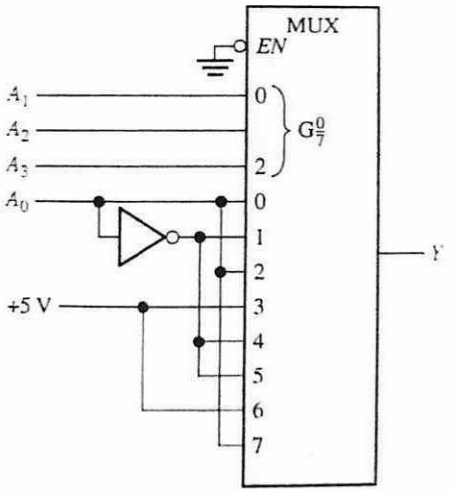

Figure Q2.1

(i) Analyze and built a truth table for **Figure Q2.1**.

(6 marks)

(ii) From your answer in part **Q2(a)(i)**, write a Boolean expression for output, Y.

(5 marks)

(b) **Figure Q2.2** show the logic symbol of 74LS138, 1-to-8 decoder. Waveform A0, A1, A2 and E3 shown in **Figure Q2.3** are applied to this decoder. Assume that $\overline{E1}$ and $\overline{E2}$ are tied to LOW (0). Draw the waveform for outputs $\overline{O0}$, $\overline{O3}$, $\overline{O6}$, and $\overline{O7}$.

(10 marks)

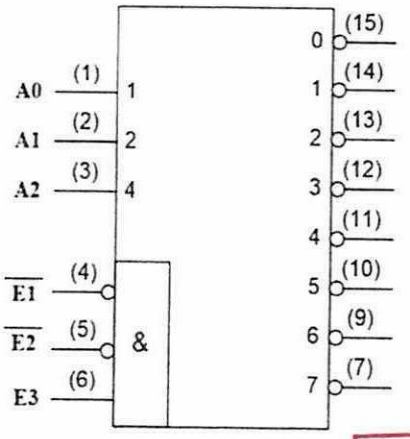

Figure Q2.2

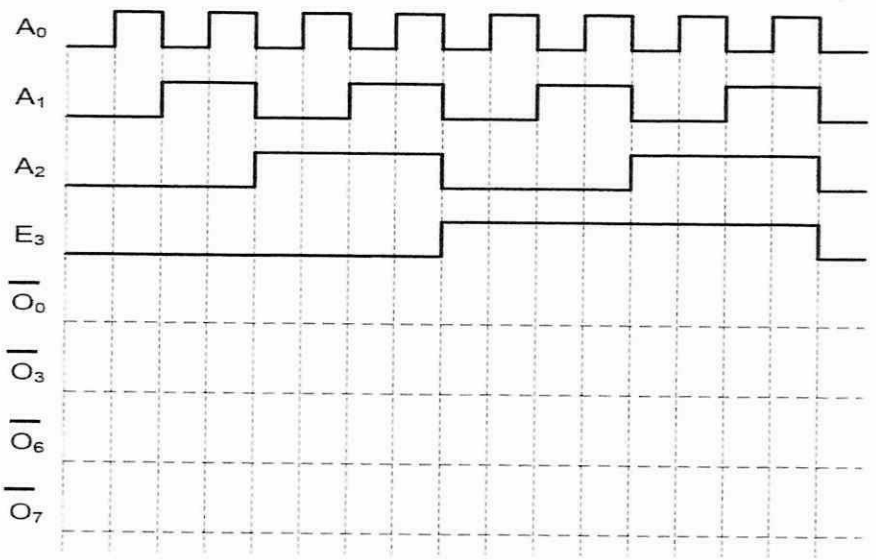

Figure Q2.3

(c) Derive the implemented logic function from a multiplexer in **Figure Q2.4**.

(4 marks)

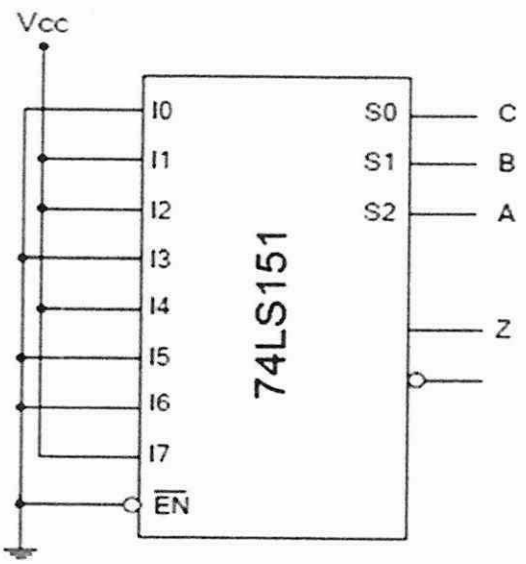

Figure Q2.4

Q3 (a) A latch is an electronic circuit with two stable states, functioning as a switch that holds and transitions between these states fundamental to digital logic and information storage.

(i) Analyze output, Q based on the timing diagram for NAND latch given in **Figure Q3.1**. Note that the initial value of Q is at LOW state.

(4 marks)

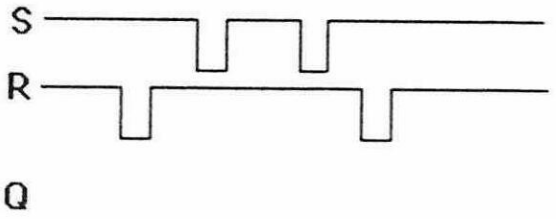

Figure Q3.1

(ii) Highlight the similarities and differences between a NAND latch and an SR flip-flop.

(4 marks)

(b) Design a clock divider using JK flip-flop that can generate frequencies of 24 kHz, and 6 kHz from input frequency of 96 kHz.

(8 marks)

(c) Given the circuit diagram in **Figure Q3.2**, determine the timing diagram for QA, QB, and QC in **Figure Q3.3**. Assume that QA, QB, and QC are in high state initially.

(9 marks)

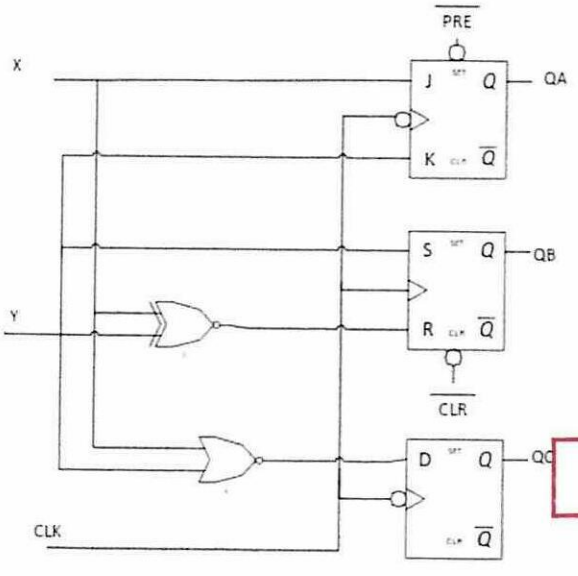

Figure Q3.2

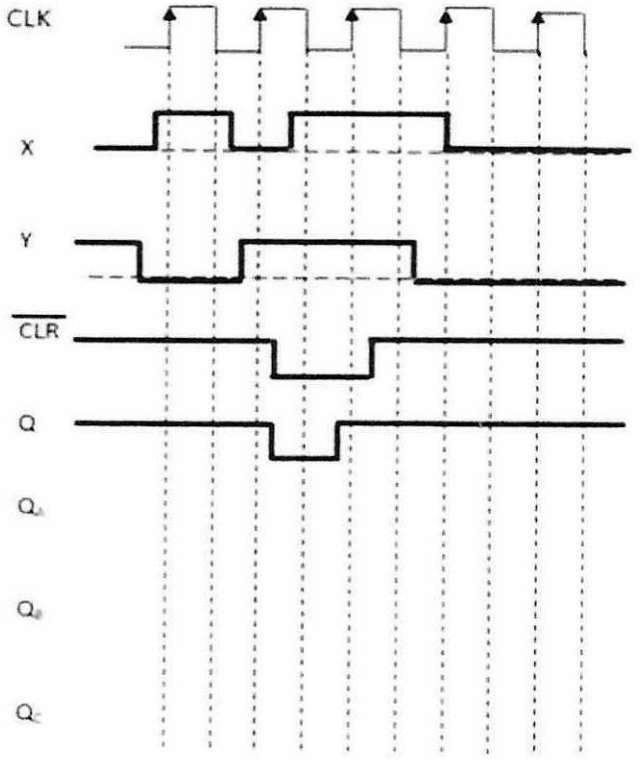

Figure Q3.3

Q4 A convocation hall in UTHM needs to be equipped with automated running light with three independent sources, L1, L2 and L3. These lights need to be controlled with close loop sequence as shown in **Figure Q4.1** to forms certain pattern. Propose a suitable state machine design to fulfil this requirement.

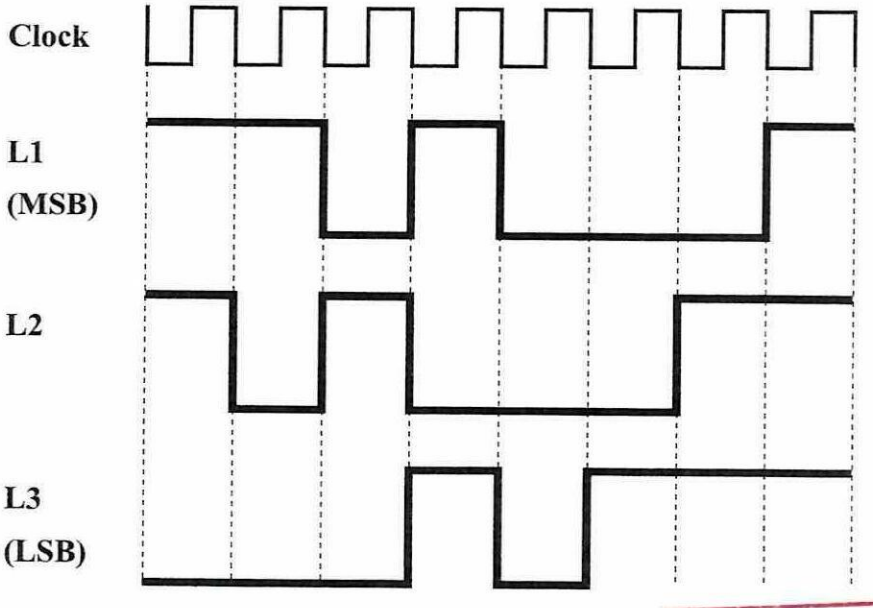

Figure Q4.1

(a) Build a state transition diagram based on **Figure Q4.1**.

(2 marks)

(b) Build the excitation table for this state machine.

(8 marks)

(c) Find the simplest Boolean expression for the circuit using Karnaugh map.

(9 marks)

(d) Implement the circuit diagram based on the result in **Q4(c)**.

(6 marks)

- END OF QUESTIONS -

APPENDIX A

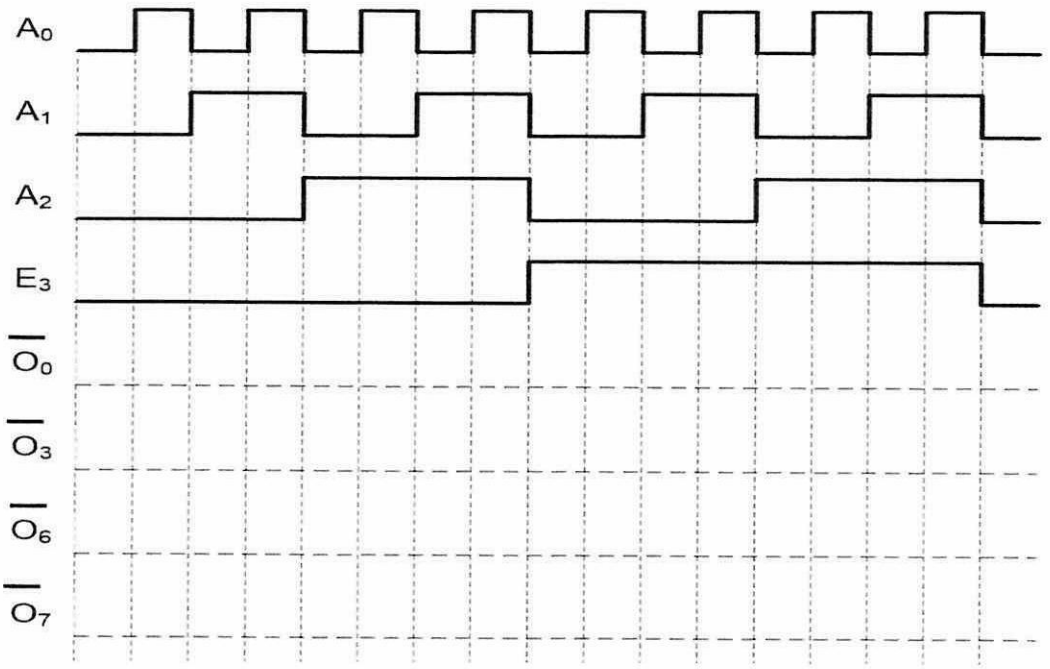

Figure Q2.3

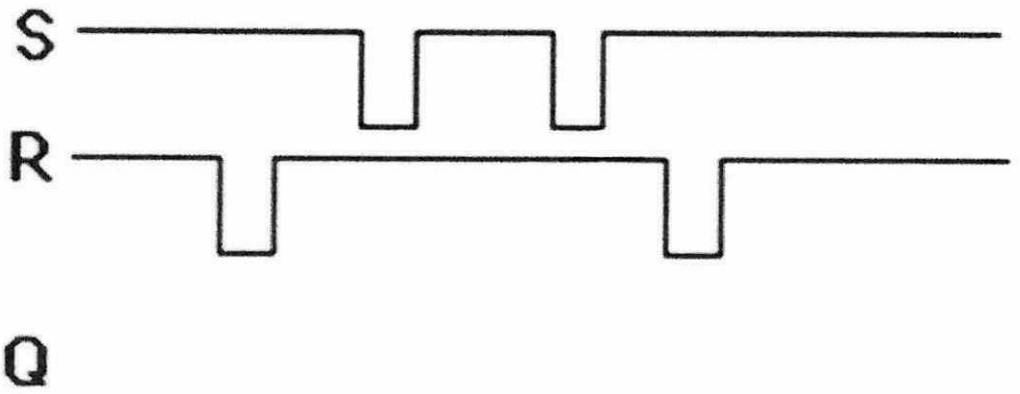

Figure Q3.1

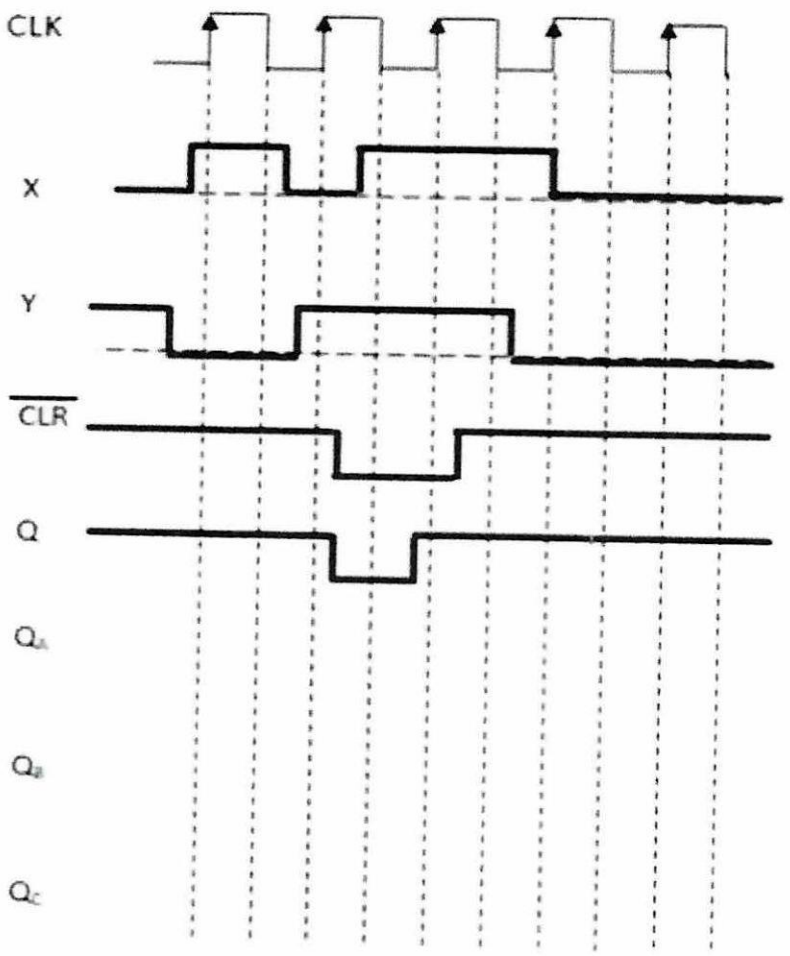

Figure Q3.3