Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER II
## SESSION 2023/2024

| | | |
|---|---|---|
| COURSE NAME | : | COMPUTER ARCHITECTURE |
| COURSE CODE | : | DAT 10703 |
| PROGRAMME CODE | : | DAT |
| EXAMINATION DATE | : | JULY 2024 |
| DURATION | : | 2 HOURS 30 MINUTES |
| INSTRUCTIONS | : | 1. ANSWER **ALL** QUESTIONS<br>2. THIS FINAL EXAMINATION IS CONDUCTED VIA<br>☐ OPEN BOOK<br>☒ CLOSED BOOK<br>3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK |

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

**PART A (20 MARKS)**

Choose the best answer.

**Q1** These devices provide a means of communication between a computer and outer world. They are often referred to as the peripheral devices sometimes.

(a) Input/ Output (I/O)
(b) Storage
(c) Compact
(d) Drivers

**Q2** Identify which of the following I/O devices does NOT use a block burst data format.

(a) Keyboard
(b) Scanner
(c) Printer
(d) Magnetic Disk

**Q3** Choose the TRUE statement about I/O devices.

(a) I/O device does have direct access to the memory unit.
(b) Each one of the instructions selects more than one I/O device by number and transfers only a single character by byte.
(c) Data transfer between the CPU and I/O devices can be done in five modes.
(d) I/O Module allow control of several different I/O devices in parallel.

**Q4** Choose the correct components constitute the number $4.1 \times 10^3$ in decimal scientific notation, which represents 4100.

(a) Mantissa of 4.1, base of 100, exponent of 3
(b) Mantissa of 4.1, base of 10, exponent of 3
(c) Mantissa of 4100, base of 10, exponent of 3
(d) Mantissa of 4.1, base of 1000, exponent of 3

**Q5** Choose the correct types of numbers on which computer arithmetic is commonly performed.

(a) Integer and complex numbers
(b) Real and imaginary numbers
(c) Floating-point and fixed-point numbers
(d) Rational and irrational numbers

**Q6** The sign magnitude representation of -1 is ....

(a) 0001
(b) 1110
(c) 1000
(d) 1001

**Q7** The bitwise complement of 0 is ....

(a) 00000001
(b) 10000000
(c) 11111111
(d) 11111110

**Q8** Select the base of the hexadecimal number system.

(a) 8
(b) 10
(c) 16
(d) 2

**Q9** Choose conversion of the decimal number 25 to binary.

(a) 11001
(b) 11010
(c) 11100
(d) 11101

**Q10** Conversion of the decimal number $0.16_{10}$ to octal is ....

(a) 0.124
(b) 0.246
(c) 0.2
(d) 0.3

**Q11** Arrange the correct hierarchy of computer languages based on **Figure Q11.**

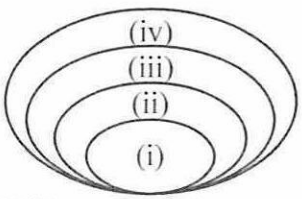


**Figure Q11** Hierarchy of Computer Languages

(a) (i) System Hardware, (ii) Assemble Language, (iii) High Level Language, (iv)Machine Language
(b) (i) High Level Language, (ii) Assemble Language, (iii) Machine Language, (iv) System Hardware
(c) (i) Machine Language, (ii) High Level Language, (iii) Assemble Language, (iv) System Hardware
(d) (i) System Hardware, (ii) Machine Language, (iii) Assemble Language, (iv) High Level Language

**Q12** .... converts the programs written in assembly language into machine instructions.

(a) Machine compiler
(b) Interpreter
(c) Assembler
(d) Converter

**Q13** Identify the correct the minimum components of an instruction in a CPU.

(a) Instruction code and memory address
(b) Opcode and data register
(c) Instruction code (opcode) and operand
(d) Memory address and data register

**Q14** Choose the correct term used to describe the encoding of instructions.

(a) Instruction layout
(b) Instruction mapping
(c) Instruction format
(d) Instruction structure

**Q15** Choose the correct difference between RISC and CISC in terms of instruction format.

(a) RISC uses variable-length encoding, while CISC uses fixed-length encoding
(b) RISC uses fixed-length encoding, while CISC uses variable-length encoding
(c) Both RISC and CISC use variable-length encoding
(d) Both RISC and CISC use fixed-length encoding

**Q16** Choose the correct category of instructions carries out calculations and includes operations like ADD, SUB, AND, OR, XOR, and SHIFT.

(a) Input/Output Instructions
(b) Control Instructions
(c) Arithmetic and Logical Instructions
(d) Data Transfer Instructions

**Q17** Choose the correct specifications and format of the Instruction Set Architecture (ISA).

(a) Only the number of instructions
(b) Number of operands, size of the operands, and order of execution
(c) Size of the operands and number of instructions
(d) Order of execution and number of instructions

**Q18** **Figure Q18** shows an assembly program that adds the values of num1 and num2 together and stores the result back into num1. Identify eax.

```
MOV eax, [num1]
ADD eax, [num2]
MOV [num1], eax
```

**Figure Q18** Assembly Program

(a) Memory
(b) Register
(c) Variable
(d) Instructions

**Q19** Identify the type of registers primarily used for storing data temporarily for processing and storing results of operations within the CPU.

(a) General-Purpose Registers
(b) Special-Purpose Registers
(c) Control Registers
(d) Index Registers

**Q20** Choose the register that is designed for a specific task within the CPU and is responsible for holding the memory address being accessed or manipulated.

(a) Program Counter (PC)
(b) Memory Data Register (MDR)
(c) Memory Address Register (MAR)
(d) Accumulator (ACC)

**PART B (80 MARKS)**

**Q21** **Figure Q21** shows the architecture of input and output. The architecture of input and output involves a coordinated effort between the central processing unit (CPU), memory, and I/O modules to facilitate the seamless flow of data into the system, processing by the CPU, and output to external devices.

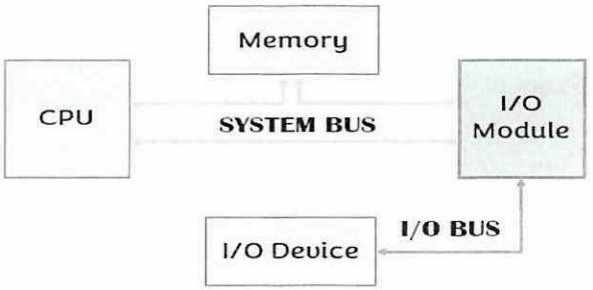


**Figure Q21** Architecture of Input and Output

(a) Explain the process involve between central processing unit (CPU), Memory and I/O Module as illustrated in **Figure Q21**.

(4 marks)

(b) Complete the following comparison **Table Q21** between the three methods of I/O handling: Programmed I/O, Interrupt Initiated I/O, and Direct Memory Access (DMA) based on the provided criteria.

**Table Q21** Comparison of three methods of I/O handling

| | Programmed I/O | Interrupt Initiated I/O | Direct Memory Access |
|---|---|---|---|
| Trigger | | | |
| Component responsible for Data Transfer | | | |
| CPU involvement (Yes/ No) | | | |
| CPU busy waiting (Yes / No) | | | |
| Direct I/O to memory access (Yes/No) | | | |

(9 marks)

(c) List the components contained within a DMA controller and describe their roles.

(3 marks)

**Q22** A CPU is an integrated circuit that is responsible for performing arithmetic, logical and I/O operations.

(a) In a diagram, illustrate the overall architecture of a CPU, including all components.
(4 marks)

(b) Differentiate between the representation of fixed-point numbers and floating-point numbers in computer arithmetic. Provide sample numbers for each.
(4 marks)

(c) Justify the usage of binary number system in digital computers.
(2 marks)

(d) Perform binary addition of 1101 and 0010.
(2 marks)

(e) Express the decimal format of the signed binary number $(101010)_2$. State the sign bit.
(3 marks)

(f) By using 2's compliment, illustrate the operation for 11 1100 + (-10 1101).

(i) Write the steps to perform the operation.
(3 marks)

(ii) State whether there any overflow or not.
(1 mark)

**Q23** A digital computer stores, understands and manipulates information consist of zeros and ones. In computing, hexadecimal or octal number systems being used to represent binary numbers.

(a) Convert the following hexadecimal numbers into binary numbers:
(i) $6B9_{16}$
(2 marks)

(ii) $6D.3A_{16}$
(2 marks)

(b) Convert the following binary numbers into decimal numbers:
(i) $11010_2$
(2 marks)

(ii) $101.1010_2$
(3 marks)

(c) Convert the following real octal numbers to its equivalent hexadecimal numbers:
(i) $536_8$
(4 marks)

(ii) $46.57_8$
(4 marks)

(d) Convert the following octal number $364_8$ to its decimal equivalent.
(3 marks)

**Q24** (a) Write instructions required to execute equation Z=X+Y using instruction format includes two operands using Load/Store through registers architecture:

(6 marks)

(b) List the advantages of "Load/Store architecture" practised in Reduced Instant set Computer (RISC).

(2 marks)

(c) Compare between Complex Instruction Set Computer (CISC) and RISC instruction sets in **Table Q24**.

**Table Q24** Comparison Between CISC and RISC

| CISC | RISC |
|---|---|
| | |
| | |
| | |
| | |
| | |

(5 marks)

**Q25** **Figure Q25** shows that the four types of the instruction cycle can be decomposed into a sequence of elementary micro-operations.

(a) Complete the instructions cycle in by naming the cycle (i), (ii),(iii) and (iv).

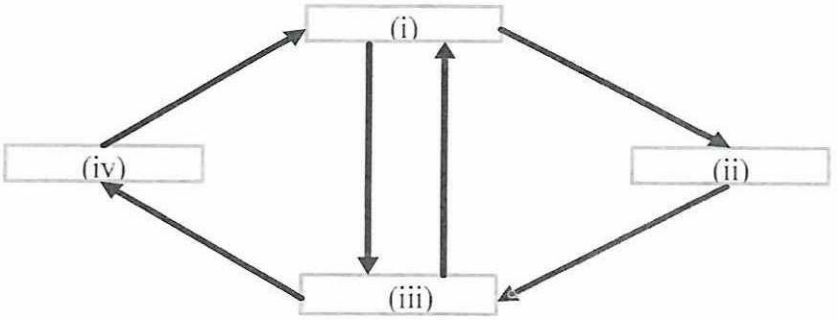


**Figure Q25** Instruction Cycle

(4 marks)

(b) Describe each phases of (i), (ii), (iii) and (iv).

(4 marks)

(c) CPU registers serves as temporary storage for immediate access of data and instructions. List **TWO (2)** types of registers and describe their roles in CPU operations.

(4 marks)

**-END OF QUESTIONS –**