Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2023/2024

COURSE NAME	:	ELECTRONICS
COURSE CODE	:	DAE 21303
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JULY 2024
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTIONS	:	1. ANSWER ALL QUESTIONS 2. THIS FINAL EXAMINATION IS CONDUCTED VIA ☐ Open book ☒ Closed book 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) With the help of diagram(s), state the concept of ideal diode which is in forward bias and reverse bias.

(4 marks)

(b) A centre-tapped full wave rectifier with a load, R_L is driven by a transformer with N_{pri} : N_{sec} turn ratio. The primary transformer is connected to a 120 Vrms, 50 Hz. The average voltage, V_{dc} that is produced by this rectifier is 27 V. Assuming diodes are ideal.

(i) Draw the schematic diagram of the circuit.

(3 marks)

(ii) Determine the transformer turns ratio.

(6 marks)

(iii) Sketch and label with values the input voltage, V_{in} and output voltage, V_o waveform of the rectifier.

(4 marks)

(iv) Calculate the Peak Inverse Voltage, PIV of each diode in the circuit.

(2 marks)

(c) Design a clamper circuit that gives a steady state input and output as shown in **Figure Q1.1**. Draw and clearly label the corresponding circuit.

(6 marks)

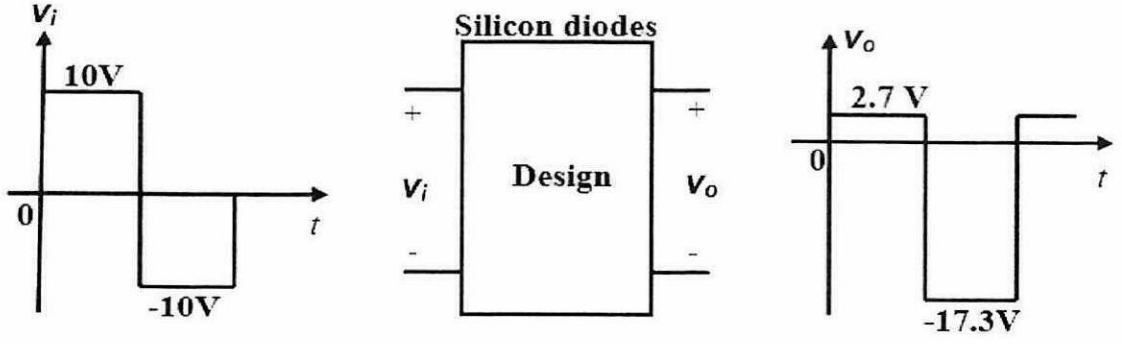

Figure Q1.1

Q2 (a) With the aid of diagram, explain the operation of zener diode.

(5 marks)

(b) Voltage regulator circuit in **Figure Q2.1** will maintain an output voltage of 20 V across a 1 kΩ load, RL with an input, V_s varies between 30 V and 50 V. Determine:

(i) The minimum, I_{Zmin} and the maximum zener current, I_{Zmax} for the network if $R_{in} = 100\ \Omega$.

(10 marks)

(ii) The zener power rating, P_{zmin} and P_{zmax}.

(4 marks)

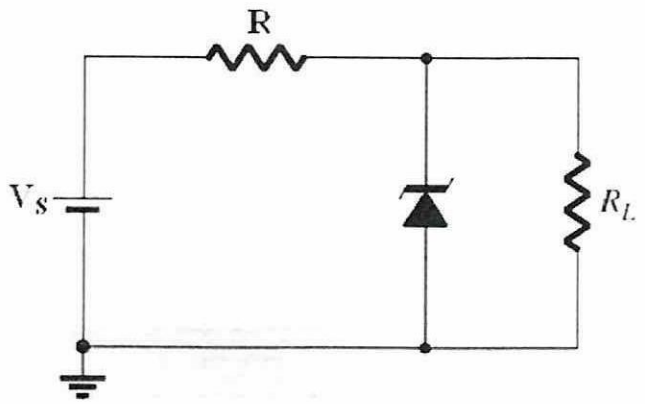

Figure Q2.1

(c) Sketch V_0 in relation to input signal in **Figure Q2.2** for at least one complete cycle. Use second approximation model and assume zener voltage for D_1 and D_2 are 3.3 V.

(6 marks)

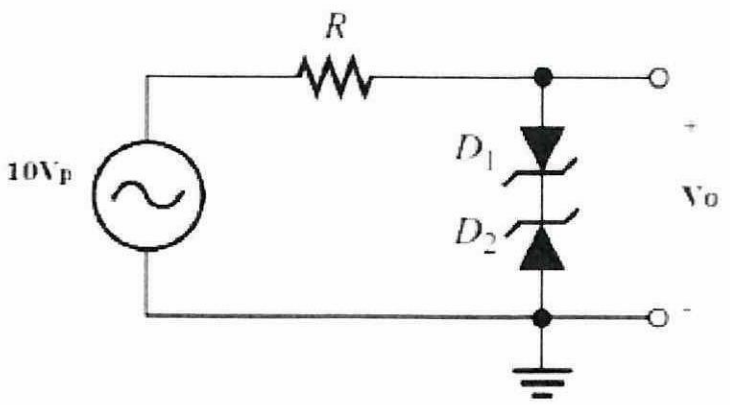

Figure Q2.2

Q3 (a) With the aid of diagrams, briefly explain the three (3) modes of operation in *npn* bipolar transistor.

(6 marks)

(b) From (a), determine which mode of operation is used as amplifier.

(1 marks)

(c) Based on the circuit configuration in **Figure Q3.1**, determine the following value;

(i) Base current and collector current, I_B and I_C.

(4 marks)

(ii) Base voltage, V_B and collector voltage, V_C.

(4 marks)

(iii) Collector-emitter voltage, V_{CE} and base-collector voltage, V_{BC}.

(4 marks)

(iv) Saturation Current, $I_{c(sat)}$

(2 marks)

(v) Cutoff value of collector-emitter voltage, $V_{CE(\ cutoff)}$

(2 marks)

(vi) Draw the load line and plot the Q-point on the resulted load line.

(2 marks)

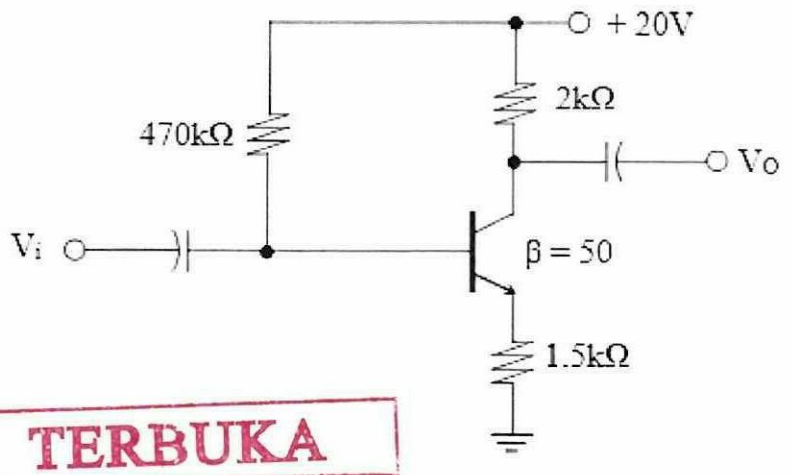

Figure Q3.1

Q4 (a) For an n-channel JFET, assume the saturation current $I_{DSS} = 2$ mA and the pinch off voltage is $V_p = -3.5$ V. Calculate I_D and $V_{DS(sat)}$ for $V_{GS} = 0$ V.

(4 marks)

(b) Sketch the transfer characteristics for an n-channel D-MOSFET with $I_{DSS} = 10$ mA and $V_p = -4$V.

(7 marks)

(c) Determine the following parameters for the network of **Figure Q4.1**.

(i) Gate-source voltage, V_{GSQ}.

(2 marks)

(ii) Drain current, I_{DQ}.

(3 marks)

(iii) Drain-source voltage, V_{DS}.

(3 marks)

(iv) Drain voltage, V_D.

(2 marks)

(v) Gate voltage, V_G.

(2 marks)

(vi) Source voltage, V_S.

(2 marks)

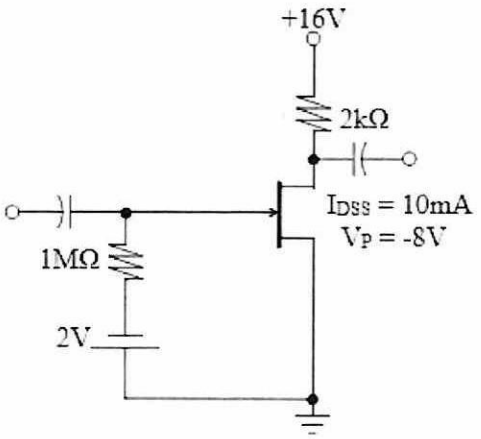

Figure Q4.1

- END OF QUESTIONS -