UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	LOGIC SYSTEMS
COURSE CODE	:	DAE 21603
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	DECEMBER 2016/ JANUARY 2017
DURATION	:	2 HOURS AND 30 MINUTES
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Explain **two** primary of logic circuit.

(3 marks)

(b) What is the difference between latche and flip-flop operation.

(3 marks)

(c) With the aid of truth tables, describe the differences between the following flip-flops

(i) RS flip flop.
(ii) JK flip-flop.
(iii) D flip-flop.

(12 marks)

(d) Given D, $\overline{\text{Preset}}$, $\overline{\text{Clear}}$ and Clok input for a D flip-flop in **Figure Q1(d).**

(i) Draw the Q output waveform

(ii) Draw the $\overline{Q}$ output waveform

(7 marks)

Q2 (a) Explain briefly two application of flip-flop.

(4 marks)

(b) For the circuit in **Figure Q2(b):**

(i) State the function of this circuit.

(2 marks)

(ii) Determine the external resistors R1 and R2 to give output frequency of 20kHz and duty cycle of 60% if the external capacitor C is 3nF.

(6 marks)

(c) **Figure Q2(c)** show JK flip-flop as a ripple counter to count up counter.

(i) Draw the timing diagram as **Figure Q2(c).**

(9 marks)

(ii) Modify the circuit to operate MOD 7 counter.

(4 marks)

Q3 (a) The logic diagram and Dual-In-Line Package for IC 7493 is given in **Figure Q3(a).** Draw the connections diagrams for the following 7493-based counters and determine the output frequency if the input clock frequency is 200 kHz. Show all steps and label the input clock as well as the outputs.

(i) MOD 9 counter
(ii) MOD 12 counter
(iii) MOD 16 counter

(15 marks)

(b) For the **Figure Q3(b)**, the propagation delay, t_{pd} for each flip-flop is 50ns And t_{pd} for AND gate is 20ns.

(i) Determine the maximum input clock frequency (f_{max}) for the Counter.
(ii) Determine the maximum input clock frequency (f_{max}) with a MOD-16 ripple counter.

(10 marks)

Q4 (a) Design a synchronous counter using JK flip-flop to count 4 digits. The count sequence is 0,2,4,6 and repeat. The JK excitation table is shown in **Table Q4(a)**. Show all steps and the design should include the following :

(i) State diagram
(ii) Circuit excitation table used to determine JK flip-flop inputs.
(iii) K-maps used to generate minimal expressions for JK inputs.
(iv) Logic circuit.

(15 marks)

(b) Explain 4 mode data movement in shift register.

(4 marks)

(c) Determine the number of flip-flops needed to construct a shift register capable of storing :

(i) a 4-bit binary number
(ii) Draw the logic diagram as a serial input/serial output shift register.

(6 marks)

Q5 (a) List **three (3)** advantages of constructing a digital circuit prototype using a PLD instead of standard logic devices.

(3 marks)

(b) Several types of architecture are used in PLDs. Draw the block diagram of three common types and describe their differences.

(6 marks)

(c) List **five (5)** limitations of PLAs.

(5 marks)

(d) Use the PLA in **Figure Q5(d)** to implement the following functions. Label all inputs and outputs.

(i) $F1(W,X,Y) = \sum(1,2,3,5,7)$
(ii) $F2(W,X,Y) = \sum(0,4,6,7)$

(11 marks)

Q6 (a) Define each basic memory operations terms below.

(i) Write
(ii) Read.
(iii) Address.

(6 marks)

(b) A certain memory has a capacity of 2K x 8, determine

(i) the number of data inputs and data outputs .
(ii) the number of address lines.
(iii) its capacity in bytes.

(9 marks)

(c) Define each of the following terms.
(i) RAM
(ii) ROM
(iii) EPROM
(iv) Internal Memory

(10 marks)

- END OF QUESTION –

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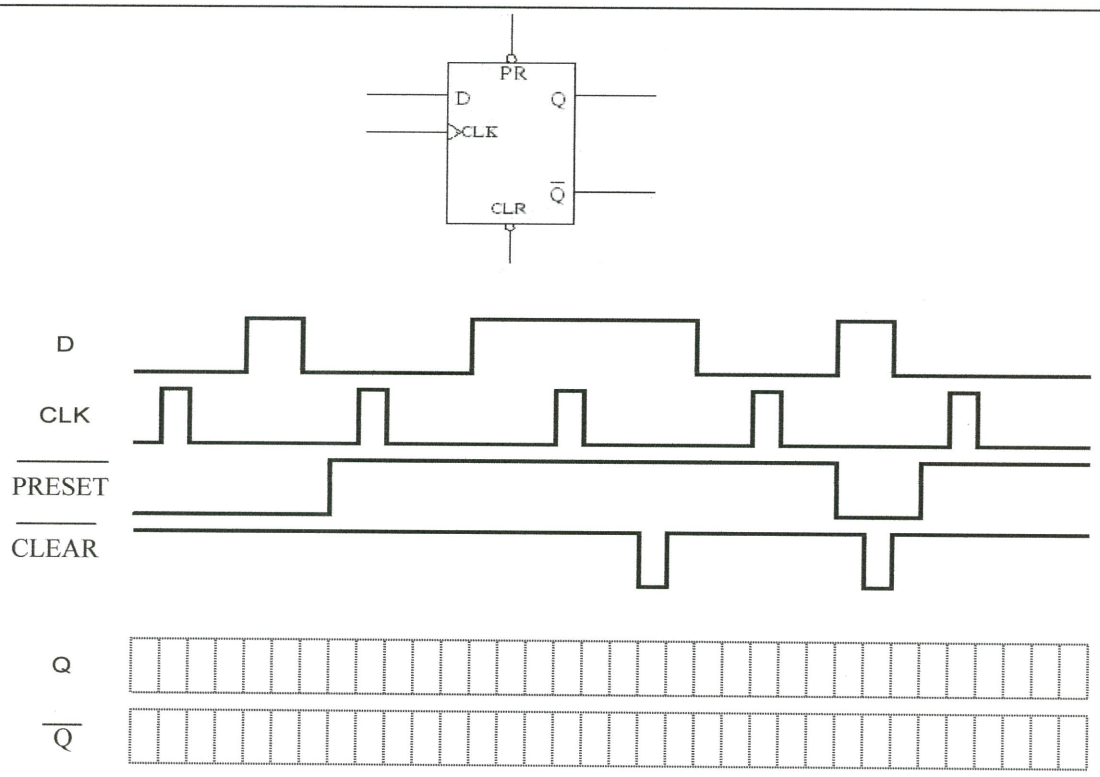

FIGURE Q1(d)

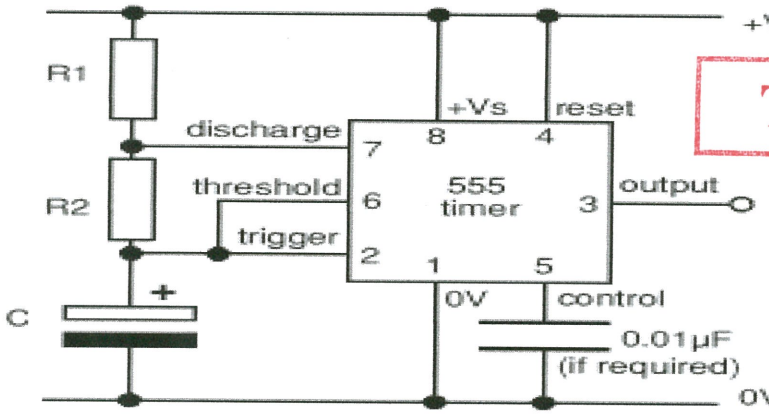

FIGURE Q2(b)

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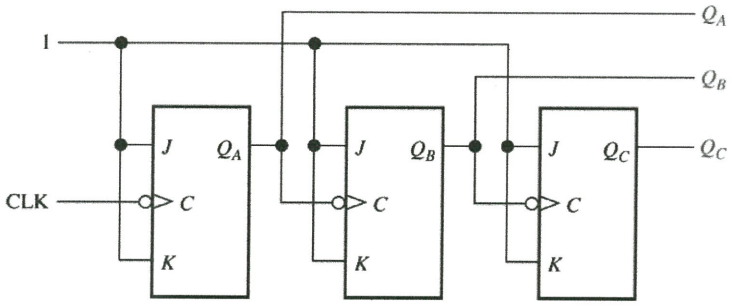

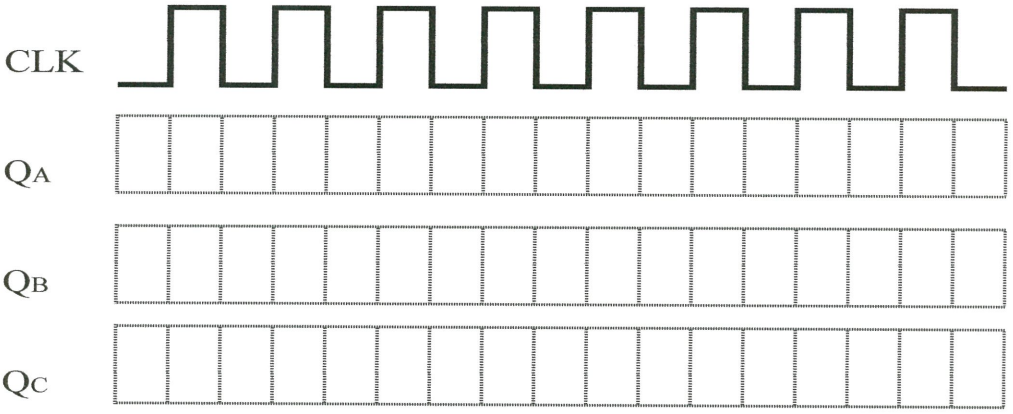

FIGURE Q2(c)

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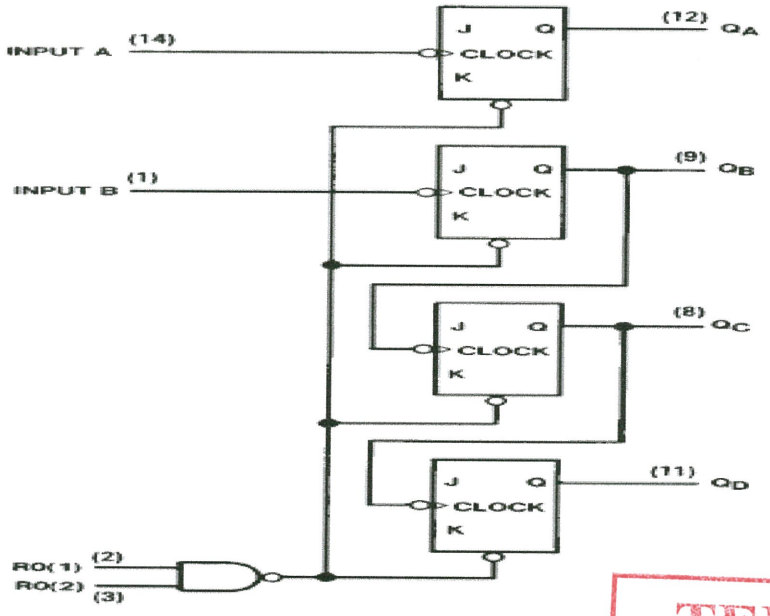

Dual-In-Line Package

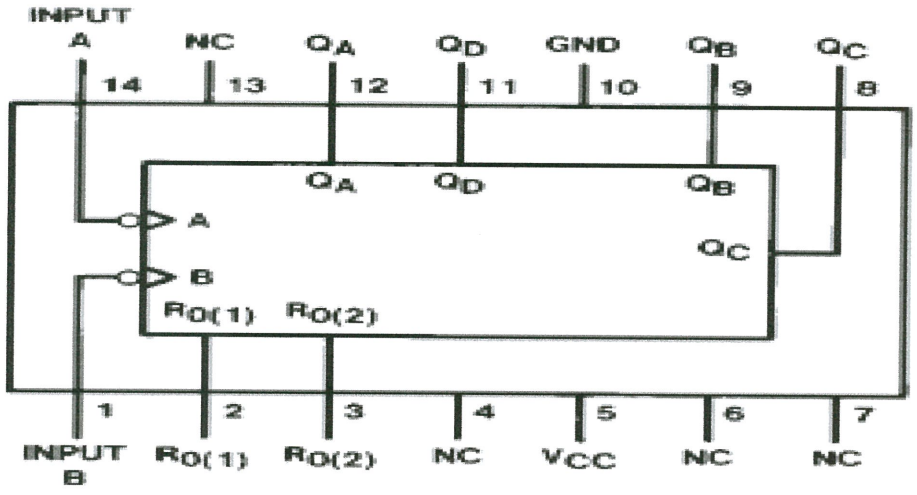

FIGURE Q3(a)

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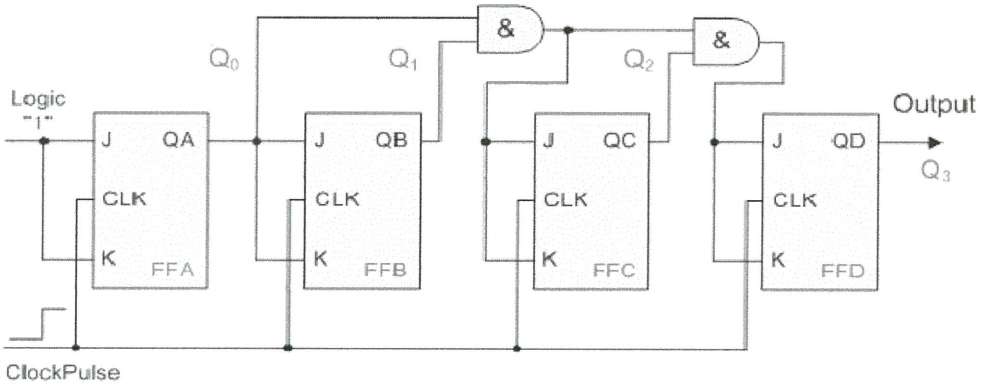

FIGURE Q3(b)

TABLE Q4(a): JK Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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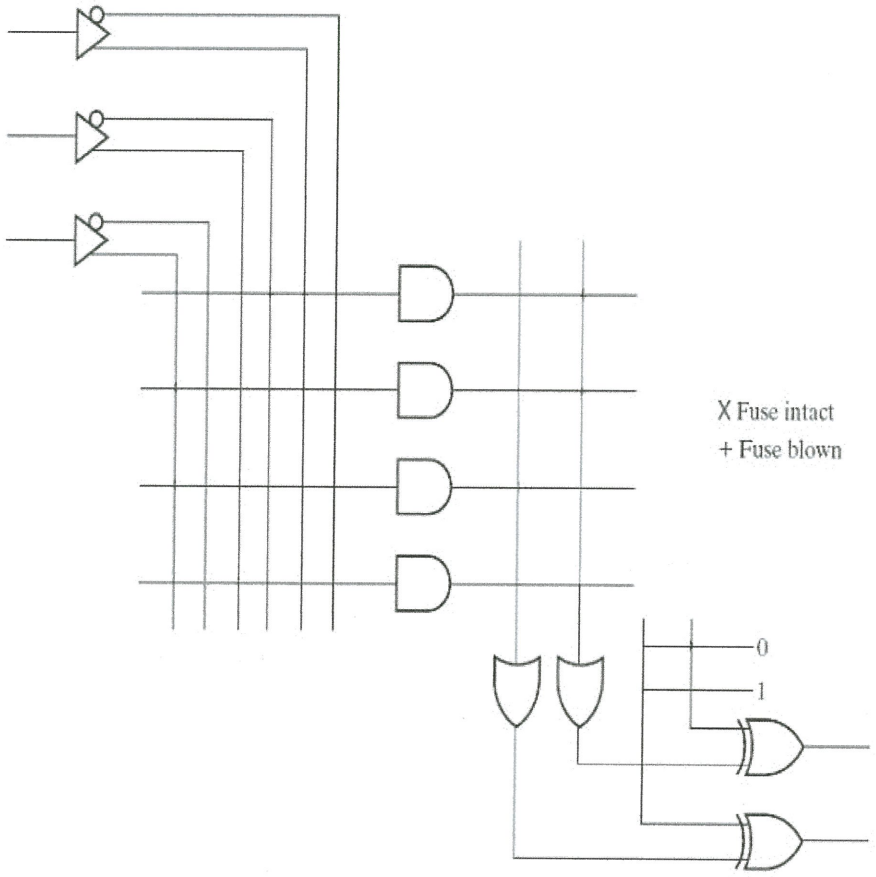

FIGURE Q5(d)