Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	ELECTRONICS
COURSE CODE	:	DAE 21303
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Describe the difference between *n*-type and *p*-type semiconductor materials.

(4 marks)

(b) Determine the current *I* for each of the configuration of **Figure Q1(b)** using 2nd approximate equivalent model for the diode.

(7 marks)

(c) A full-wave bridge rectifier with a 120 V_{rms} sinusoidal input has a load resistor of 1 kΩ.

(i) If silicon diodes are employed, what is the dc voltage available at the load?
(ii) Determine the required PIV rating of each diode.
(iii) Find the maximum current through each diode during conduction.
(iv) What is the required power rating of each diode?

(8 marks)

(d) **Figure Q1(d)** shows a clamper circuit. Analyze and sketch the output voltage V_o. Assume that V_k for Ge is 0.3 V.

(6 marks)

Q2 (a) Name and explain **three (3)** applications of diodes.

(6 marks)

(b) With the aid of a block diagram, explain briefly the functions of each block of a basic power supply unit and sketch the waveforms at each output if the input is a sinusoidal waveform.

(11 marks)

(c) For the zener diode network of **Figure Q2(c)**. Determine

(i) The load voltage, V_L
(ii) The load current, I_L
(iii) The series resistor current, I_R
(iv) The zener diode current, I_Z

(8 marks)

Q3 (a) In what **two (2)** states of operation when a transistor is used as a switch?

(2 marks)

(b) Draw the output characteristic (I_C versus V_{CE}) for the common-emitter configuration. Then using these curves, show where the three operating regions of the transistor.

(5 marks)

(c) A transistor has the following currents: Emitter current $I_E = 3.2$ mA and base current $I_B = 20$ μA. Solve for α_{dc}, β_{dc} and collector current I_C.

(6 marks)

(d) Draw a DC load line for the transistor circuit in **Figure Q3(d)** and indicate the values of $I_{C(sat)}$, $V_{CE(off)}$, I_{CQ}, and V_{CEQ} on the load line.

(12 marks)

Q4 (a) Determine the following for the voltage divider configuration of **Figure Q4(a)**.

(i) The dc base current, I_B
(ii) The dc collector current, I_C
(iii) The dc collector-emitter voltage, V_{CE}
(iv) The dc emitter voltage, V_E
(v) The dc base voltage, V_B
(vi) The dc collector voltage, V_C

(12 marks)

(b) For the amplifier circuit shown in **Figure Q4(b),** draw the ac equivalent circuit using hybrid model and determine the followings if $\beta = 200$:

(i) The input impedance, Z_i
(ii) The output impedance, Z_o
(iii) The voltage gain, A_V
(iv) The output voltage, v_o

(13 marks)

Q5 (a) For the JFET self-bias common-source amplifier of **Figure Q5(a)**,

(i) Sketch the transfer curve for the device.
(ii) Superimpose the network equation on the same graph.
(iii) Determine I_{DQ} and V_{GSQ}.
(iv) Calculate V_{DS}, V_D, V_G, and V_S.

(15 marks)

(b) For the JFET Voltage-Divider common-source amplifier of **Figure Q5(b).** Determine the followings if V_{GSQ} = - 0.95 V:

(i) Input impedance, Z_i
(ii) Output impedance, Z_o
(iii) Output voltage, V_o if V_i = 20 mV

Given :

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

(10 marks)

Q6 (a) With the aid of diagrams, state and explain the **two (2)** conditions of oscillation.
(6 marks)

(b) For the oscillator circuit in **Figure Q6(b),** determine the:

(i) frequency of oscillation
(ii) feedback factor, β and the value of the voltage gain, A_v.
(iii) new value of L for the circuit to oscillates at 800 kHz.

(8 marks)

(c) The 555 timer of **Figure Q6(c)** has R_1 = 20 kΩ, R_2 = 10 kΩ, and C = 0.047 μF.

(i) Calculate the frequency of the output signal.
(ii) Determine the duty cycle
(iii) Draw the output waveform

(11 marks)

- END OF QUESTION -

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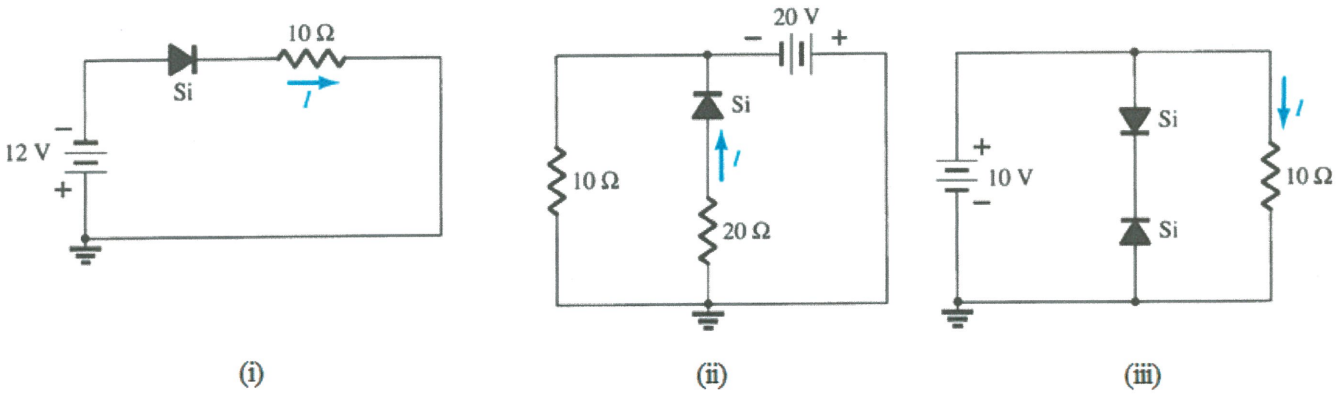

Figure Q1(b)

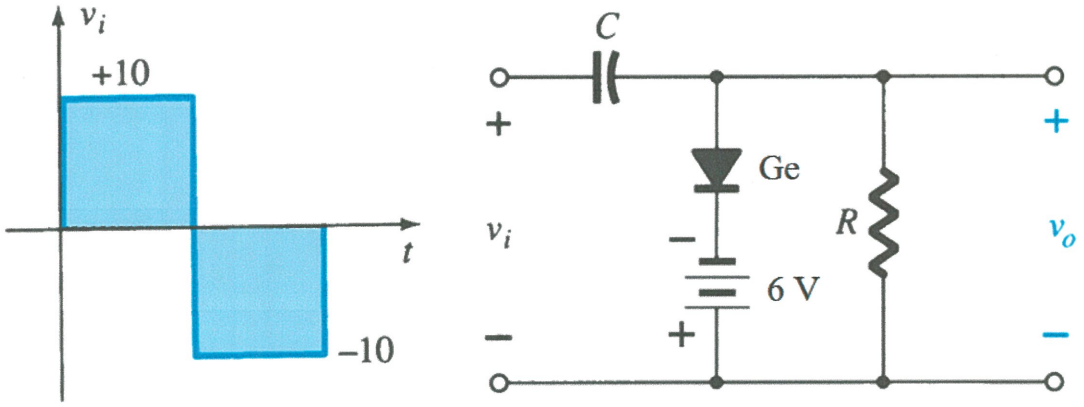

Figure Q1(d)

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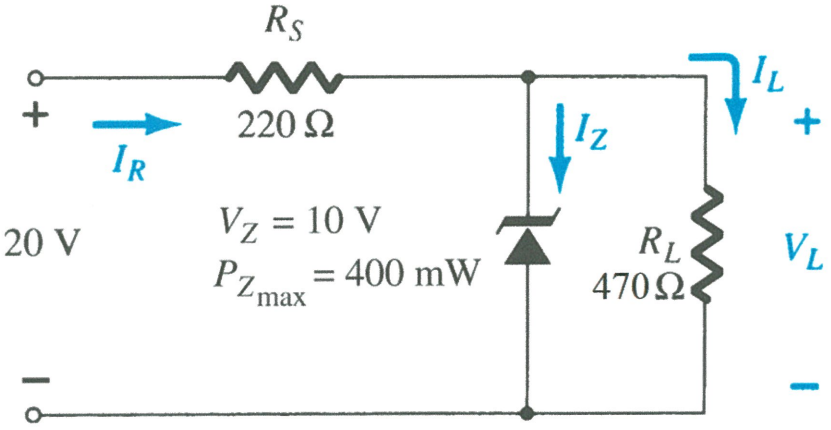

Figure Q2(c)

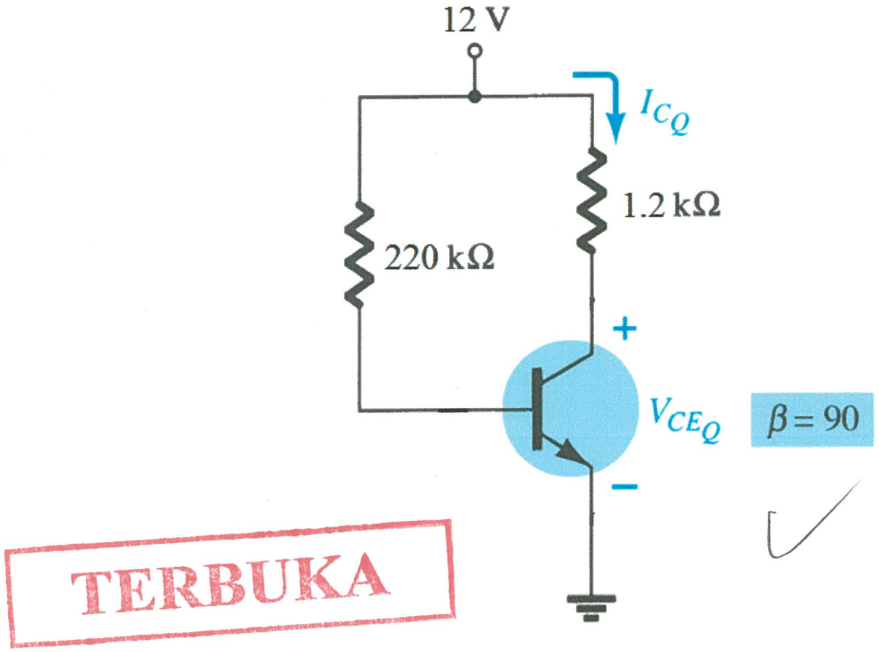

Figure Q3(d)

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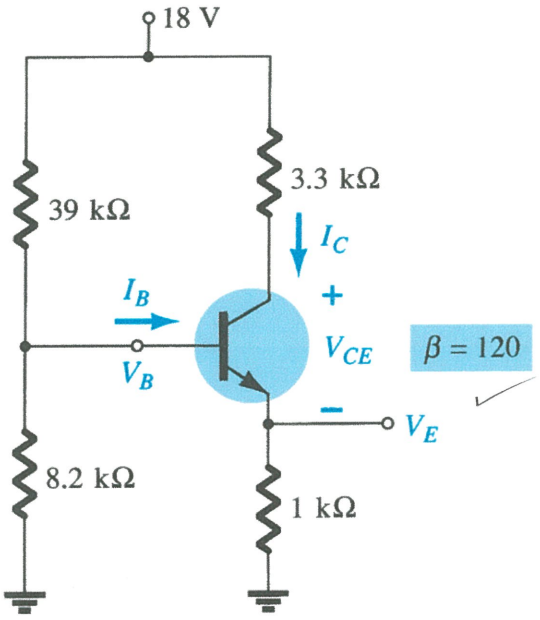

Figure Q4(a)

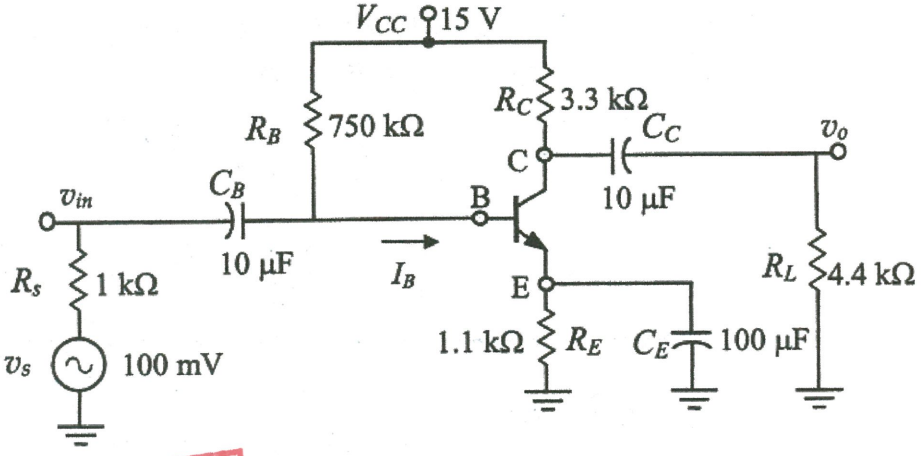

Figure Q4(b)

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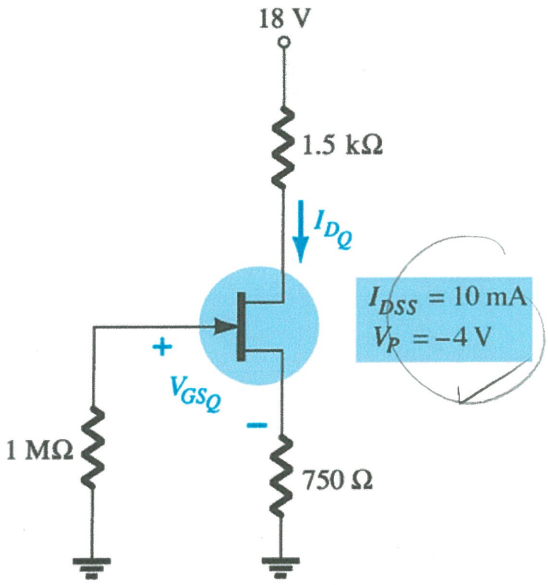

Figure Q5(a)

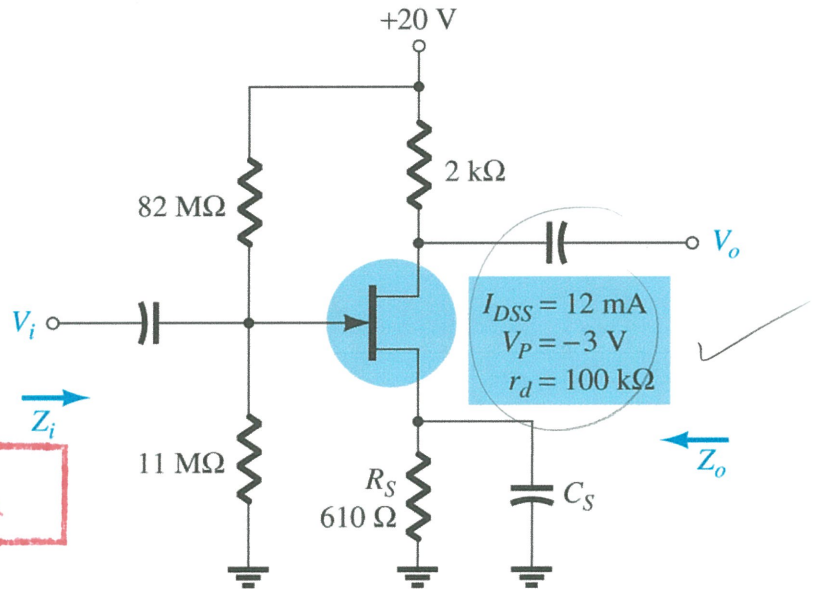

Figure Q5(b)

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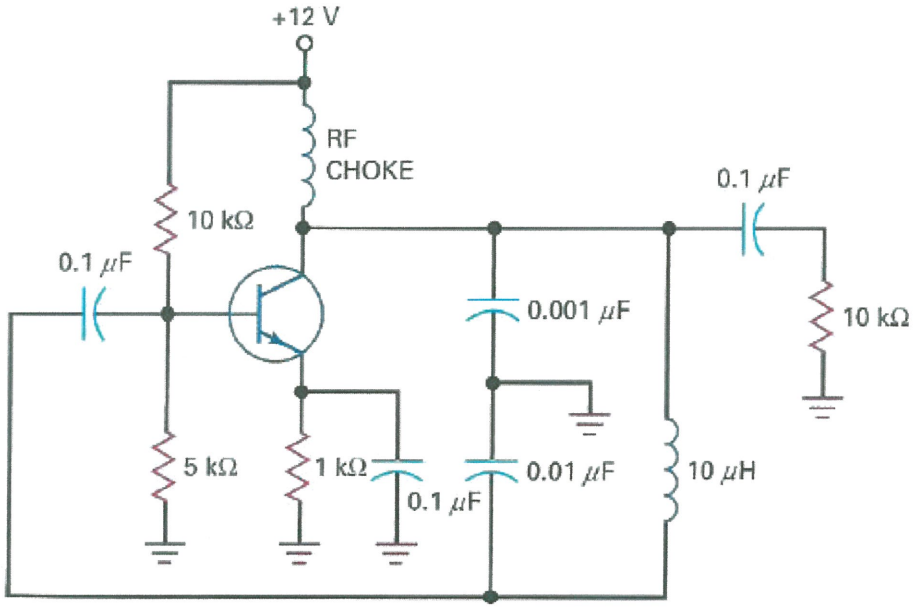

Figure Q6(b)

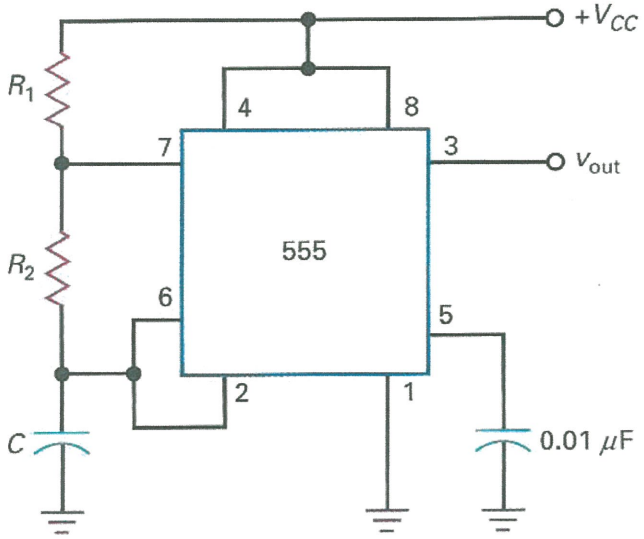

Figure Q6(c)