UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2023/2024

COURSE NAME   :   ELECTRONICS

COURSE CODE   :   DAE 21303

PROGRAMME CODE   :   DAE

EXAMINATION DATE   :   JANUARY/ FEBRUARY 2024

DURATION   :   3 HOURS

INSTRUCTIONS   :   1. ANSWER ALL QUESTIONS
                            2. THIS FINAL EXAMINATION IS CONDUCTED VIA
                               ☐ Open book
                               ☒ Closed book
                            3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

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Q1 (a) With the help of diagram(s), state the concept of an ideal diode which is in forward bias and reverse bias.

(2 marks)

(b) Each diode in **Figure Q1 (b)** is a complete model diode with a threshold voltage equal to V_T. Diode D_1 and D_2 are germanium diodes with $V_T = 0.3$ V whereas D_3 and D_4 are silicon diodes with $V_T = 0.7$ V.

(i) For $R = 10$ kΩ, calculate V_o, V_R, I_R, I_1 and I_2.

(5 marks)

(ii) Evaluate V_o, V_R and I_R if diode D_1 and D_2 are removed from the circuit. Use $R = 10$ kΩ.

(3 marks)

(iii) What happens when the polarity of the battery is reversed? Calculate V_o.
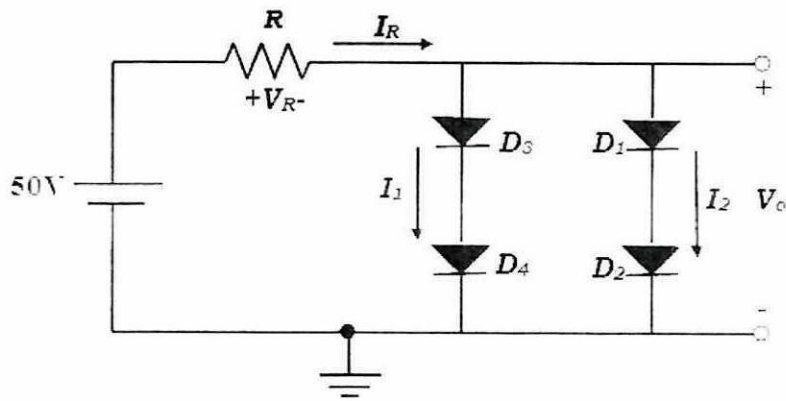
(2 marks)

Figure Q1 (b)

(c) Design a clamper circuit that gives a steady state input and output as shown in **Figure Q1 (c)**. Draw and clearly label the corresponding circuit.
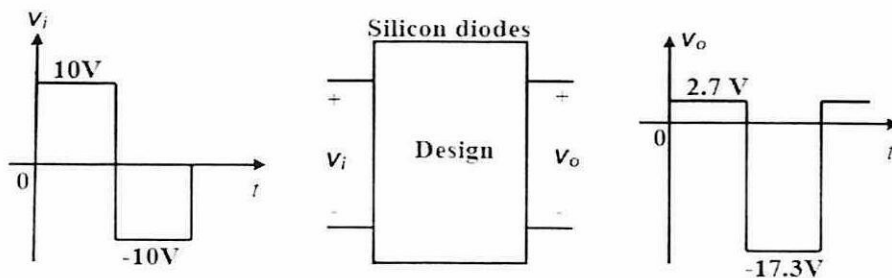
(8 marks)

Figure Q1 (c)

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Q2 (a) A full-wave bridge rectifier with a load, R_L is driven by a transformer with $N_{pri} : N_{sec}$ turns ratio. The primary transformer is connected to a 240 V_{rms}, 60 Hz. The average voltage, V_{dc} that is produced by this rectifier is 35 V. Assuming diodes are silicon.

(i) Draw the schematic diagram of the circuit.

(3 marks)

(ii) Determine the transformer turns ratio.

(3 marks)

(iii) Sketch and label with values the input voltage, V_{in} and output voltage, V_o waveform of the rectifier.

(3 marks)

(iv) A capacitor filter of 1mF is then connected to the output of the rectifier in part Q2 (a). Calculate the new average filtered voltage if the load current is 0.1 A.

(4 marks)

(b) Zener regulator is a combination of elements designed to ensure the output voltage of a supply remains constant fairly. For the Zener regulator circuit depicted in **Figure Q2 (b)**. determine the followings if $R_L = 220 \, \Omega$.

(i) The load voltage and load current. V_L and I_L.

(2 marks)

(ii) The source current, I_R and Zener current, I_Z.

(2 marks)

(iii) Does the zener diode in part Q2 (b)(i and ii) conduct? If not, select the minimum load, R_L that will turn the Zener diode ON.
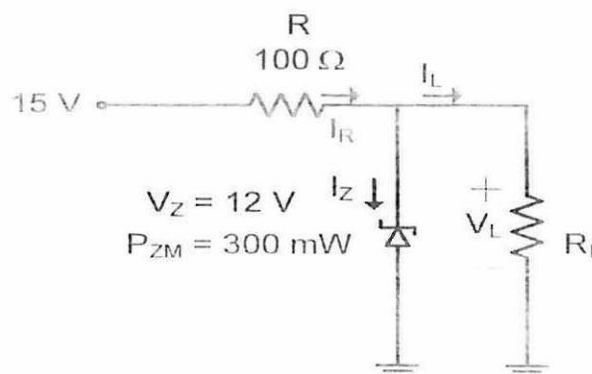
(3 marks)

Figure Q2 (b)

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Q3 (a) With the help of diagrams, briefly explain the three modes of operation in *NPN* bipolar transistor. Which mode of operation is used in an amplifier?

(4 marks)

(b) Based on the circuit configuration in **Figure Q3 (b)**, determine the following value;

(i) Base current and collector current, I_B and I_C.

(4 marks)

(ii) Base voltage, V_B and collector voltage, V_C.

(4 marks)

(iii) Collector-emitter voltage, V_{CE} and base-collector voltage, V_{BC}.

(2 marks)

(iv) Saturation Current, $I_{c\ (sat)}$

(2 marks)

(v) Cutoff value of collector-emitter voltage, $V_{CE(\ cutoff)}$

(2 marks)

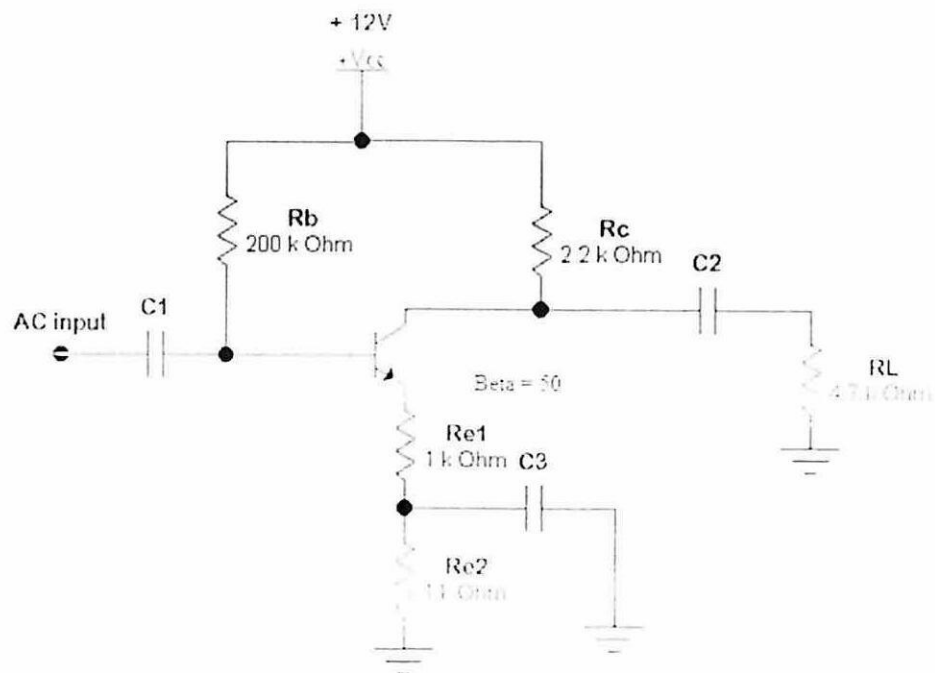(vi) Draw the load line and plot the Q-point on the resulted load line.

(2 marks)

Figure Q3 (b)

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Q4   For the common-emitter amplifier shown in **Figure Q4**, solve the items below.

(a)   Determine the AC emitter resistance, r_e.

(5 marks)

(b)   Draw the AC equivalent circuit with complete labelling.

(2 marks)

(c)   Determine the input impedance, Z_i with $r_0 = \infty \ \Omega$

(1 mark)

(d)   Determine the output impedance, Z_0 with $r_0 = \infty \ \Omega$

(1 mark)

(e)   Determine the voltage gain, A_V with $r_0 = \infty \ \Omega$

(2 marks)

(f)   Determine the current gain, A_i with $r_0 = \infty \ \Omega$

(2 marks)

(g)   Recalculate **Q4 (d)** until **Q4 (f)** with $r_0 = 50 \ k\Omega$

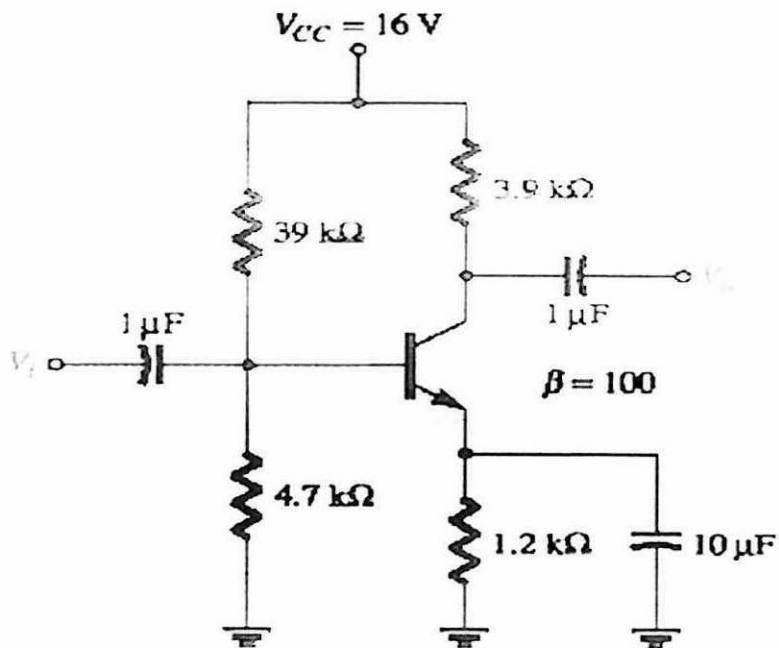(3 marks)

(h)   Analyze your results in **Q4 (g)**.

(4 marks)

Figure Q4

Q5 (a)   A self-bias circuit configuration of a n-channel JFET has the following parameters:
V_{DD} = 20 V, R_D = 6.2 kΩ, R_G = 1 MΩ and R_S = 2.4 kΩ.

  (i)   Sketch and label the circuit configuration.

(2 marks)

  (ii)   Using data in **Table Q5**, sketch the transfer characteristic curve.

(3 marks)

  (iii) Identify the drain-source saturation current, I_{DSS}, and the pinch-off voltage, V_p.

(2 marks)

  (iv)   Analyze the circuit and determine the Q-point, I_{DQ} and V_{GSQ}.

(4 marks)

Table Q5 : Data for transfer characteristic curve

I_D (mA)	0	0.5	2	4.5	8	12.5
V_{GS} (V)	-8	-6	-4	-2	0	2

 (b)   A JFET Voltage-divider amplifier circuit with I_{DSS} = 9 mA and V_p = -4.5 V, has an operating point defined by V_{GSQ} = -1.8 V and I_{DQ} = 5.4 mA. Assume the value of Y_{os} is given as 20 µS, R_{G1} = 15 kΩ, R_{G2} = 5 kΩ, R_D = 3 kΩ and R_S = 2 kΩ.

  (i)   Sketch the AC equivalent circuit with complete labelling. Hence, determine the transconductance, g_m and output drain-source resistance, r_d.

(4 marks)

  (ii)   Calculate the input and output impedance, Z_i and Z_o.

(3 marks)

  (iii) Find the midband voltage gain, A_v.

(2 marks)

- END OF QUESTIONS -

APPENDIX

$I_E = I_C + I_B$

$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$

$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$

$A_i = -A_v \dfrac{Z_i}{R_C}$

$I_D = I_{DSS} \left(1 - \dfrac{V_{GS}}{V_P} \right)^2$

$r_d = \dfrac{1}{y_{os}}$

$g_m = \dfrac{2 I_{DSS}}{|V_P|} \left[1 - \dfrac{V_{GS}}{V_P} \right]$

$g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$

$\dfrac{A_v}{-g_m} = (r_d || R_D)$

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