Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	DAE 21203
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	JULY / AUGUST 2023
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS
		2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK**
		3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **SIXTEEN (16)** PAGES

PART A: ANSWER ALL QUESTIONS IN THE OMR FORM (30 MARKS)

Q1 Which one of the following logical operations is performed by the digital circuit shown in **Figure Q1**?

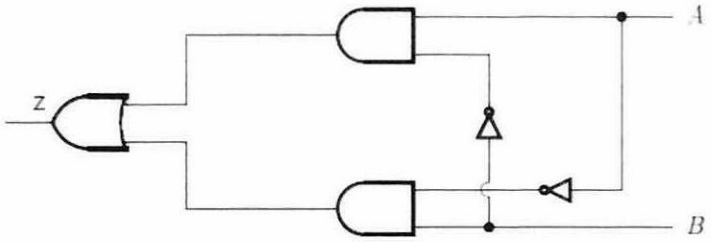


Figure Q1

A. z = NOR
B. z = XOR
C. z = NAND
D. z = XNOR

Q2 The truth table of a circuit is shown in **Table Q2**. The expression for $\bar{X}$ is

Table Q2

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0

A. $AB + \bar{B}C + B\bar{C}$
B. $\bar{B}C$
C. $\bar{B}C + AB\bar{C}$
D. $AB\bar{C}$

Q3 In the circuit of **Figure Q3**, the output Z is

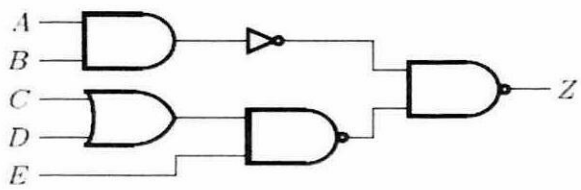


Figure Q3

A. $AB + (C + D)E$
B. $AB + CD + E$
C. $AB(C + D)E$
D. $AB + CDE$

Q4 The switching circuit given in the **Figure Q4** can be expressed in binary logic notation as

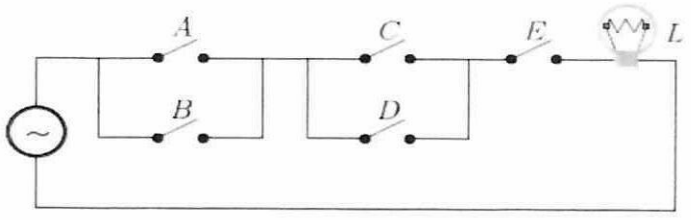


Figure Q4

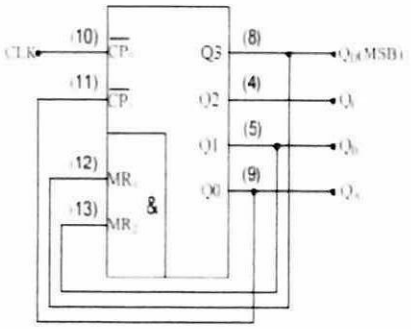
A. $L = (A + B)(C + D)E$
B. $L = AB + CD + E$
C. $L = E + (A + B)(C + D)$
D. $L = (AB + CD)E$

Q5 Parallel data can be taken out of a shift register simultaneously with the method of;

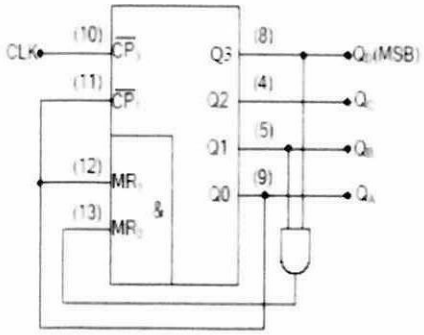
A. Use the Q output of the first FF.
B. Use the Q output of the last FF.
C. Tie all of the Q outputs together.
D. Use the Q output of each FF.

Q6 Which of the following shows the connection for MOD-6 counter?

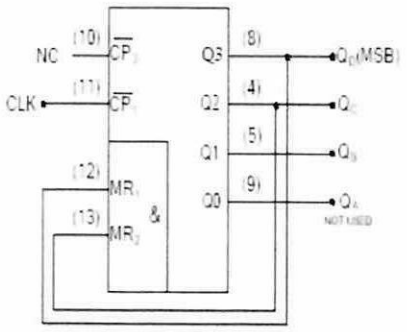
A.



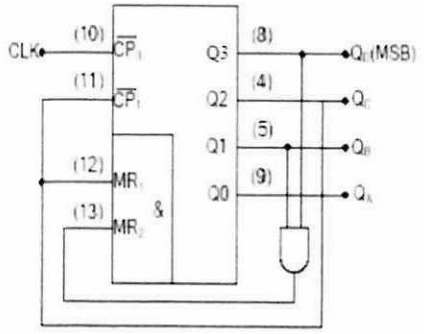
C.



B.



D.



Q7 When a serial data transmission sends data from a computer to a modem, the least significant bit is sent first. What is the data received at the modem if the data is 01001110?

A. 01001110
B. 01100010
C. 01110010
D. 01011110

Q8 Investigate which the following input and output value are **incorrect** for the 4-bit parallel binary adder/subtractor circuit in the **Figure Q8**?

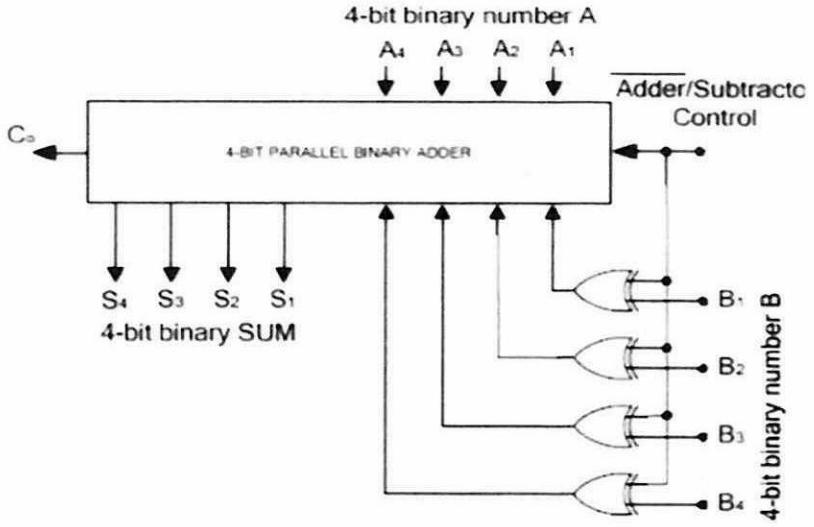


Figure Q8

	[A]	[B]	$\overline{\text{Adder/Subtractor}}$	Cout	[Σ]
A.	1101	0110	0	1	0011
B.	1001	1000	0	1	0001
C.	1111	1011	1	1	0100
D.	0101	1000	1	0	1011

Q9 What is the difference between a LATCH and a FLIP-FLOP?

A. Latch is a level sensitive device while flip-flop is an edge sensitive device.
B. Latches take less gates (also less power) to implement than flip-flops.
C. Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches.
D. All of above

Q10 The binary representation of BCD code 00101001_{BCD} is

A. 0011101_2
B. 0110101_2
C. 1101001_2
D. 0101011_2

Q11 What is a device shown in the **Figure Q11**?

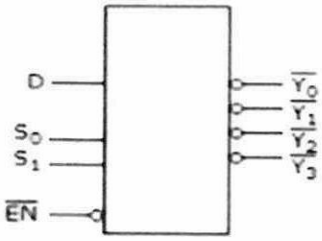


Figure Q11

A. Comparator
B. Multiplexer
C. Inverter
D. Demultiplexer

Q12 To expand a 4 bit parallel adder to an 8 bit parallel adder you must

A. use 4 bit adders with no connections.
B. use eight 4 bit adders with no interconnections.
C. use two 4 bit adders and connect to the sum outputs of one to the bit output of the other.
D. use two 4 bit adders with the carry output of one connected to the carry input of the other.

Q13 If a 74LS85 magnitude comparator has A = 1011 and B = 1001 on the inputs, the outputs are:

A. A>B = 0, A<B = 1, A=B = 0
B. A>B = 1, A<B = 1, A=B = 0
C. A>B = 1, A<B = 0, A=B = 0
D. A>B = 0, A<B = 0, A=B = 1

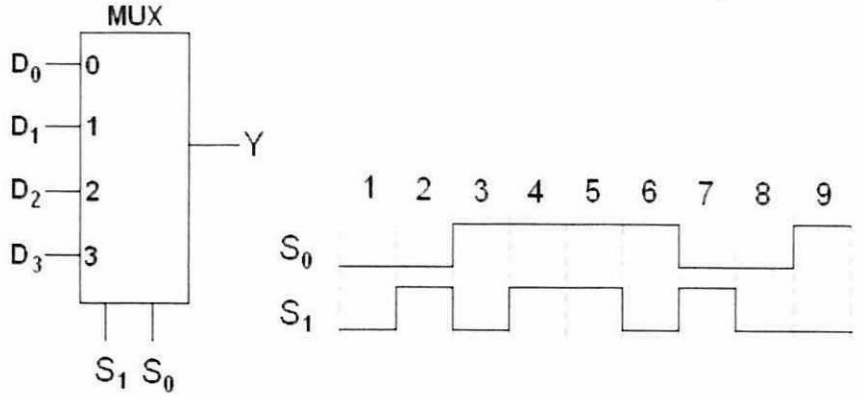
Q14 With regard to a D latch, _____.

A. the Q output follows the D input when EN is LOW
B. the Q output is opposite the D input when EN is LOW
C. the Q output follows the D input when EN is HIGH
D. the Q output is HIGH regardless of EN's input state

Q15 Table shown is a truth table for a 4-to-2 line priority encoder. Which of the inputs and outputs combination is **correct**?

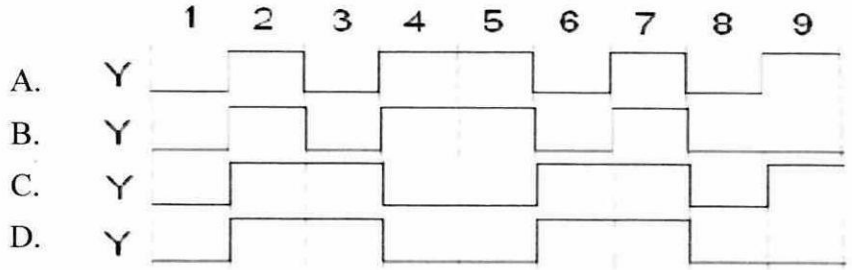
	Inputs					Outputs	
	En	D0	D1	D2	D3	A1	A0
A.	0	0	0	0	1	x	x
B.	1	1	0	0	1	0	0
C.	1	0	1	0	1	0	1
D.	1	0	0	1	1	1	1

Q16 The following data input has been applied to the multiplexer shown in **Figure Q16(a)**: D_0=0, D_1=1, D_2=1, and D_3=0. The data-select inputs to the multiplexer are sequenced as shown by the waveforms in **Figure Q16(b)**, determine the output waveform.



(a) **(b)**

Figure Q16



Q17 The full-adder shown by the **Figure Q17** is tested under all input conditions with the input waveforms shown. From your observation of the SUM and C_{OUT} waveforms, is it operating properly, and if not, what is the most likely fault?

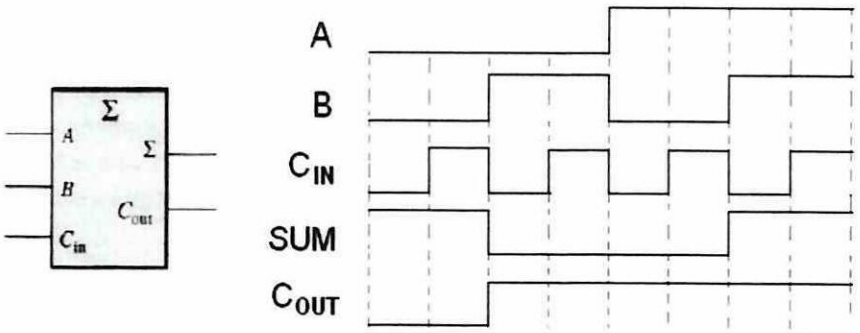


Figure Q17

A. Yes, the output SUM and C_{OUT} are correct.

B. No, the input B is accidentally connected to V_{CC}.

C. No, the input C_{IN} is accidentally connected to V_{CC}.

D. No, the input A is accidentally connected to V_{CC}.

Q18 Procedure for the design of combinational circuits are:

I. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
II. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
III. Simplify the switching expression(s) for the output(s).
IV. Implement the simplified expression using logic gates.
V. Write down the switching expression(s) for the output(s).

A. II, III, IV, V, I
B. I, IV, V, II, III
C. I, II, V, III, IV
D. I, II, III, IV, V

Q19 Consider the statements below.

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.
2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement, which is always true, is

A. Both 1 and 2
B. Only 1
C. 2
D. None of the above

Q20 Which of the following expressions is in the product-of-sums form?

A. $(A + B)(C + D)$
B. $(AB)(CD)$
C. $AB(CD)$
D. $AB + CD$

Q21 Determine the value of 10111100_2 if it is expressed in 2's complement form.

A. -68_{10}
B. -67_{10}
C. -60_{10}
D. -66_{10}

Q22 On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when

A. the clock pulse is LOW
B. the clock pulse is HIGH
C. the clock pulse transitions from LOW to HIGH
D. the clock pulse transitions from HIGH to LOW

Q23 The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially cleared. What are the Q outputs after two clock pulses?

A. 0000
B. 0010
C. 1000
D. 1111

Q24 When an invalid condition in the operation of an active-HIGH input S-R latch occurs?

A. HIGHs are applied simultaneously to both inputs S and R
B. LOWs are applied simultaneously to both inputs S and R
C. a LOW is applied to the S input while a HIGH is applied to the R input
D. a HIGH is applied to the S input while a LOW is applied to the R input

Q25 Consider the given circuit diagram in **Figure Q25** of switching of light from two different switches. The input conditions needed to turn on LED is

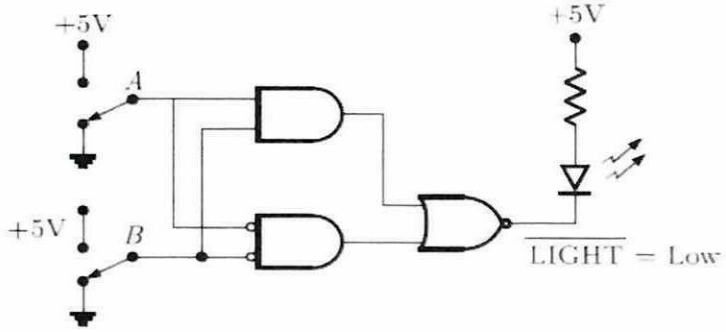


Figure Q25

A. $A = B = 1$
B. $A = 1; B = 0$
C. $A = B = 0$
D. Both (A) and (B)

Q26 The elevator door should open if the elevator is stopped, it is at the same level with the floor, and the timer has not expired, or if the elevator is stopped, it is at the same level with the floor, and a button is pressed.

If D = Elevator door opens; S = Elevator is stopped; F = Same level with the floor; T = Timer expired; B = Button pressed.

Which of the following Boolean expression represents the above condition?

A. $D = SF\bar{T} + SFB$
B. $D = SF + \bar{T}B$
C. $D = SF\bar{T}B$
D. $D = (S + F)\,\bar{T}B$

Q27 Which of these flip – flops cannot be used to construct a serial shift register?

A. D
B. SR
C. T
D. JK

Q28 In a natural food restaurant, fruit is offered for desert but only in certain combination. One choice is either orange or apple or both. Another choice is either mango and apple or neither. A third choice is orange, but if you choose orange, then you must also take banana. If the fruits are represented by their first alphabet of the name, then the logical expression that specifies the fruit available for desert in the simplified form is

A. $A + B$
B. $A + O$
C. $M + O$
D. $M + B$

Q29 A copy machine generate of a stop sign *S*, to stop the machine operation and energize and indicates light if according to either of the following conditions exists:

(1) There is no paper in the paper feeder tray.
(2) The two micro switch in the paper path are activated, indicating a jam in the paper path.

The presence of paper in the feeder tray is indicated by a high at logic signal *P* as shown in **Figure Q29**. Which of the following represents the correct logic circuit so as to get HIGH output at *S*?

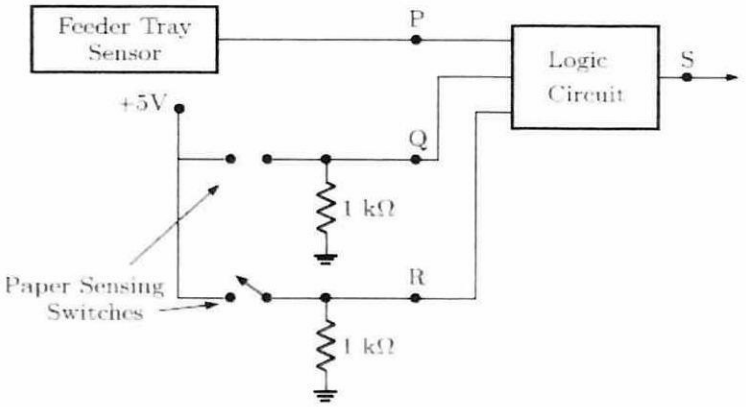
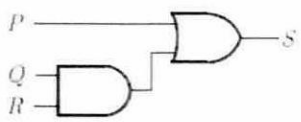
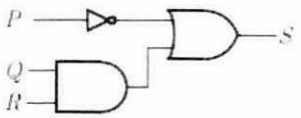
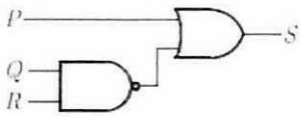
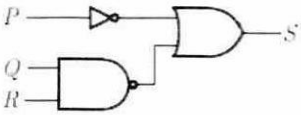


Figure Q29

A. 

C. 

B. 

D. 

Q30 In the circuit of **Figure Q30** the output *Z* is

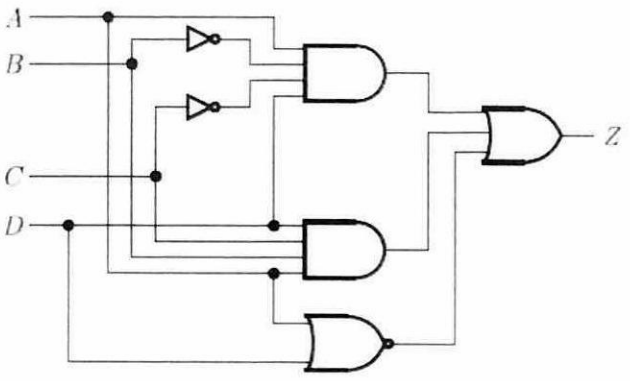


Figure Q30

A. $AD(B + C) + \overline{A}\,\overline{D}$
B. $AD(\overline{B} \oplus \overline{C}) + \overline{A}\,\overline{D}$
C. $AD(B \oplus C) + \overline{A}\,\overline{D}$
D. $\overline{A}\,\overline{D}(B \oplus C) + AD$

PART B: ANSWER ALL QUESTIONS IN THE QUESTION BOOKLET (70 MARKS)

Q1 A design of a food ordering system with combinational logic circuit has three inputs B, C, S and three outputs P, Q and R. Each input represents an item that a person may order. The items are;

- B stands for burger, which cost $3.
- C stands for cake, which cost $1.
- S stand for soda, which cost $2.

Each input can only be 1 or 0, which means that a customer can order each item only once (or none at all, for B=0, C=0, S=0). The outputs P, Q and R represent a 3-bit encoding of the total cost of the order. For example, for B=1, C=1 and S=0 (which evaluate to $4), the output should be P=1, Q=0 and R=0.

(a) Obtain the truth table for this combinational logic circuit.

(8 marks)

ANSWER:

(b) Determine the minimum expression for P, Q and R in SOP form by using K-Map

(8 marks)

ANSWER:

(c) Draw the combinational logic gates for the food ordering system

(4 marks)

ANSWER:

Q2 (a) **Figure Q2(a)** shows a shaft encoder system that measures the angle rotation in rotating machine. The encoder consists of a disc with the fixed pattern shown in **Figure Q2(a)** rotating in the anti-clockwise direction. Three light sources are used to shine light through each of three concentric rings on the encoder and are detected by the three photo detectors on the other side of the encoder disc. The most inner ring encodes the least significant bit (LSB) of the angle. In this way, one revolution is divided into 8 separate segments where segment 0 is from 0° to 45°, segment 1 is from 45° to 90°, and so on up to and including segment 7. Light cannot penetrate through the shaded region of the disc. Each photo detector produces logic '1' if light is detected and a logic '0' if otherwise.

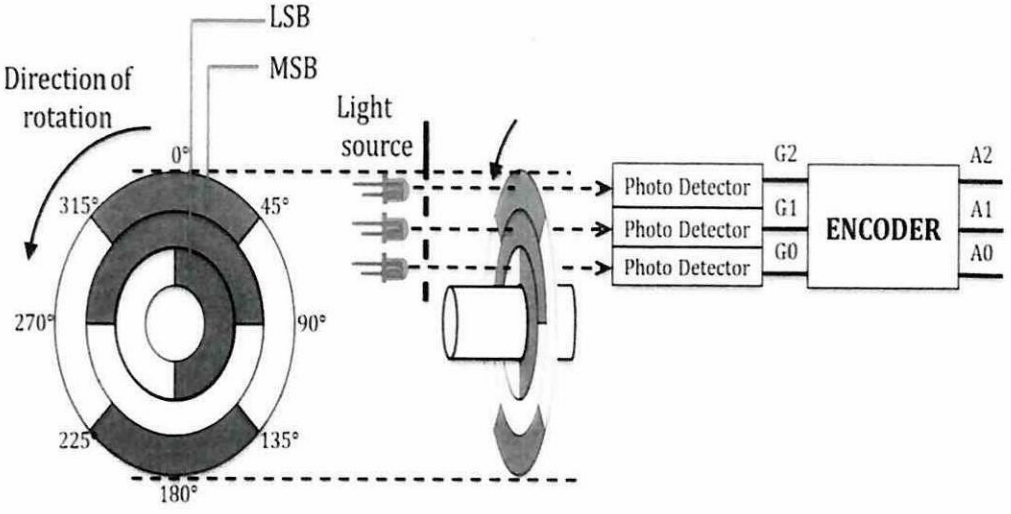


Figure Q2(a)

(i) Derive the truth table showing the segment and the corresponding signals *G2*, *G1* and *G0*.

(7 marks)

ANSWER:

(ii) Obtain the simplest Boolean expressions for *A2*, *A1* and *A0*.

(6 marks)

ANSWER:

(b) Circuit in **Figure Q2(b)**has three inputs (A, B and C) and one output (Z), connected to a multiplexer IC74151 (refer to the pin assignment). Fill in the truth table shown in **Table Q2(b)** for the output, Z, and its SOP expression.

(6 marks)

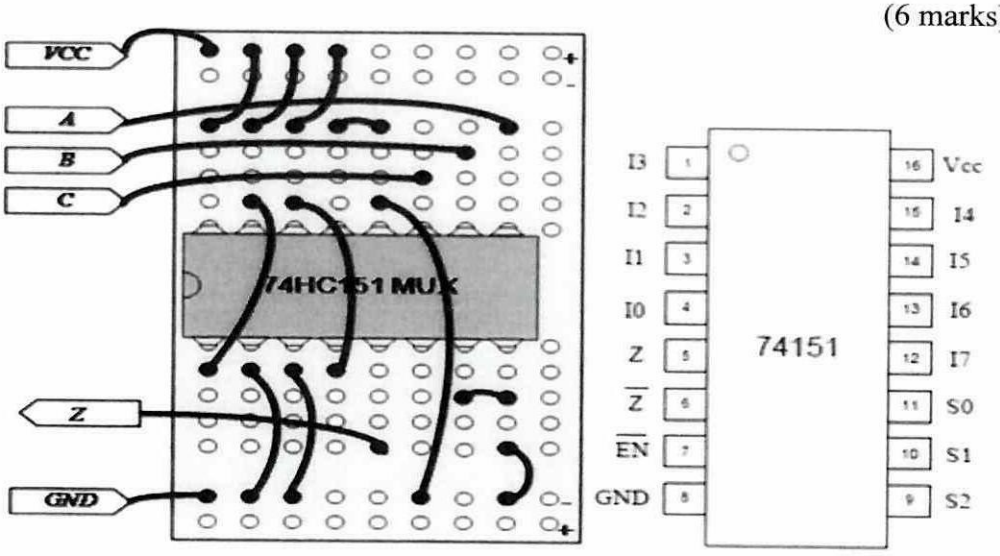


Figure Q2(b)

ANSWER:

Table Q2(b)

INPUTS

			Z
0	0	0	
1	1	1	

$Z =$ _____

(c) Given the functions of $W = A\bar{B}\bar{C} + C$, and $Y = AC + AB + \bar{A}B\bar{C}$. Using one (1) decoder IC74138 shown in **Figure Q2(c)(i)**, implement both logic funtion for W and Y. Draw the circuit by using **Figure Q2(c)(ii)**.

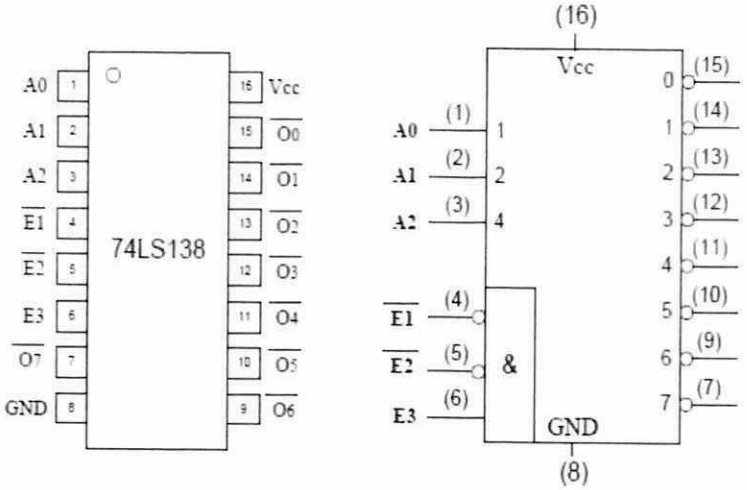


Figure Q2(c)(i)

(6 marks)

ANSWER:

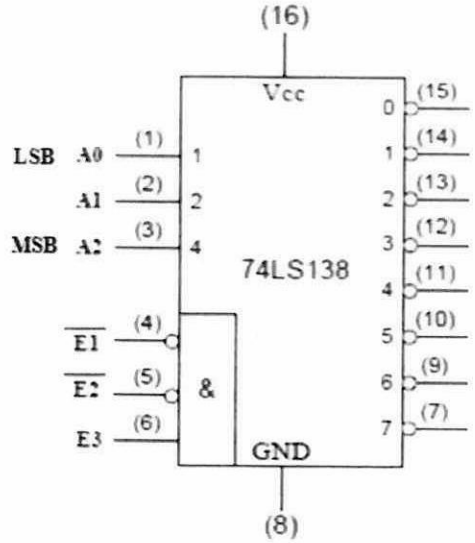


Figure Q2(c)(ii)

Q3 (a) Given J, K, $\overline{PRESET}$, $\overline{CLEAR}$ and *NGT-Clk* input waveforms for a JK flip-flop as shown in **Figure Q3(a)**, sketch for output $\bar{Q}$.

(7 marks)

ANSWER:

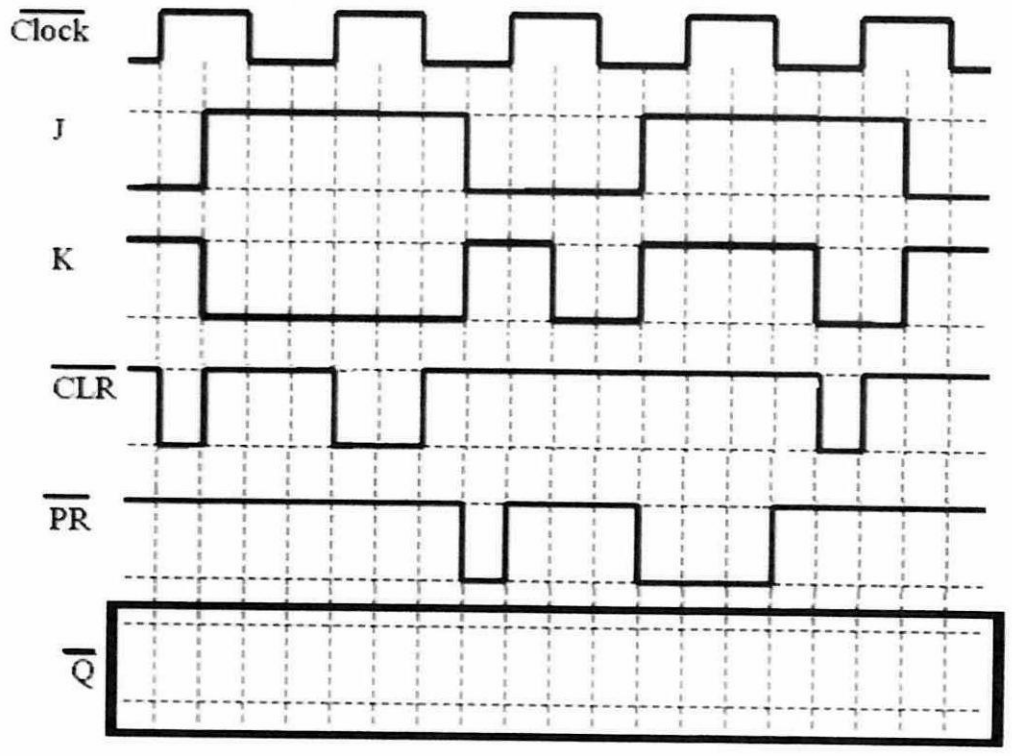


Figure Q3(a)

(b) Design an asynchronous down counter using JK flip-flop counting from 111_2 to 010_2 and label the circuit completely.

(7 marks)

ANSWER:

(c) Obtain the Boolean expression of a synchronous counter using JK flip-flop to count sequence of $11_2 \rightarrow 01_2 \rightarrow 10_2 \rightarrow 00_2$ and repeat. The JK excitation table is shown in **Table Q3(c)**. Show all steps and the design should include the following:

Table Q3(c): JK FF's Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(i) State diagram and excitation table.

(6 marks)

ANSWER:

(ii) K-maps to generate simplified expression.

(5 marks)

ANSWER:

- END OF QUESTIONS –