Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	DAT 10703
PROGRAMME CODE	:	DAT
EXAMINATION DATE	:	JULY / AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTIONS	:	1. ANSWER **ALL** QUESTIONS
		2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.**
		3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

SECTION A (20 MARKS)

Q1 Fill in the blanks with the correct answer.

a) Networking between systems was invented during _____ computer generation.

b) The fifth computer generation was utilized to develop _____ software.

c) A bus consists of multiple communication pathways known as _____.

d) Computers that rely on physical memory tend to be _____ than computers using virtual memory.

e) _____ bus link registers and various internal parts of the CPU together.

f) Devices made for the older and slower ISA bus standard are connected via a _____ controller chip.

g) I/O system requires system bus, ports and _____.

h) I/O modules that control a single type of device are often called device _____.

i) Arithmetic Unit performs calculations related to addition, subtraction and _____.

j) _____ register contains the address of the current program instruction or the next instruction to be executed.

k) The processor fetches instructions from _____ one at a time.

l) The processing required for a single instruction is called an instruction _____.

m) _____ bus carries signals from a single specific source to a single specific destination.

n) _____ bus requires addressing signals on the bus to identify the desired destination that is being pinpointed by the source at a particular time.

o) _____ replaces IDE and is used primarily as an interface for magnetic and optical disk storage devices.

p) Devices that can be added and removed at any time without powering down the system are known as _____.

q) PCIe is designed as a high-speed replacement for the PCI and _____ standards.

r) _____ bus requires a system shut down for the device to be detected by the computer.

s) Hexadecimal number system uses _____ hexadecimal digit.

t) A part in an instruction which specifies the operation to be performed is known as _____.

SECTION B (80 MARKS)

Q2 (a) Compare between RISC and CISC instruction sets by filling in **Table Q2(a)**.
(5 marks)

(b) Calculate the number of instructions cycles required to perform the calculation in **Figure Q2(b)**.
(1 mark)

(c) Examine the category of opcode involved for calculation in **Q2(b)**.
(2 marks)

(d) Determine the instructions involved for calculation in **Q2(b)**.
(3 marks)

(e) Convert the calculation in **Q2(d)** into mnemonics.
(3 marks)

(f) Explain **TWO (2)** disadvantages of the RISC instruction set.
(2 marks)

Q3 (a) Determine the registers required for the instruction in **Figure Q3(a)**.
(3 marks)

(b) Interpret the output of the instruction set in **Q3(a).**
(1 mark)

(c) List **SEVEN (7)** registers available in the CPU.
(7 marks)

(d) Explain **FIVE (5)** types of registers available in the CPU.
(5 marks)

(e) Explain **THREE (3)** conditions the program execution will halt.

(3 marks)

Q4 (a) Explain how memory devices are organized into a hierarchy based on the locality of reference.

(1 mark)

(b) Determine **FOUR (4)** criteria which affect the USB drive classification in the memory hierarchy.

(4 marks)

(c) List **ONE (1)** example of a memory device from each level of the memory hierarchy by filling in **Table Q4(c)**.

(3 marks)

(d) Describe the processes of the memory access cycle by filling in **Table Q4(d)**.

(8 marks)

(e) Conclude **THREE (3)** benefits of storing data on hard disk instead of USB drive according to the memory hierarchy level.

(3 marks)

(f) Compare internal memory and external memory by filling in **Table Q4(f)**.

(4 marks)

Q5 (a) Sketch the architecture of input and output system.

(3 marks)

(b) Explain why I/O module is required in I/O architecture.

(2 marks)

(c) Explain **FIVE (5)** characteristics of Interrupt Initiated I/O.

(5 marks)

(d) Compare Programmed I/O and Direct Memory Access by filling in **Table Q5(d)**.

(5 marks)

(e) Explain **FOUR (4)** benefits of having separate I/O controllers by filling in **Table Q5(e)**.

(4 marks)

(f) Explain **THREE (3)** possible forms which the I/O module could be.

(3 marks)

-END OF QUESTIONS –

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Table Q2(a)

CISC	RISC

```
totalDays = totalWeeks x 7
```

Figure Q2(b)

Memory

200	1 5 1 2	Load 512
201	5 5 1 3	Add 513
202	2 5 1 4	Store 514
512	0 1 4 3	
513	0 0 0 1	
514	0 0 5 0	

Figure Q3(a)

Table Q4(c)

Memory Level	Example

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Table Q4(d)

Cycle	Description

Table Q4 (f)

	Internal Memory	External Memory
Storage capacity		
Physical form / Material		

Table Q5 (d)

	Programmed I/O	Direct Memory Access
Trigger		
Component responsible for Data Transfer		
CPU involvement (Yes/ No)		
CPU busy waiting (Yes / No)		
Direct I/O to memory access (Yes/No)		

Table Q5 (e)

Benefit	Explanation