Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA
FINAL EXAMINATION
SEMESTER II
SESSION 2022/2023

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEJ30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY/AUGUST 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ANSWER SECTION A IN OMR FORM 3. ANSWER SECTION B IN THIS BOOKLET 4. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.** 5. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK.

THIS QUESTION PAPER CONSISTS OF **NINETEEN (19)** PAGES

SECTION A: OBJECTIVE QUESTIONS (50 MARKS)

Q1 Which register is used to store the value of arithmetic and logical operation?

a) Accumulator
b) Address Register
c) Arithmetic register
d) Index Register
e) Data register

(1 mark)

Q2 What is the effective address for ADD 2(R3, R4)

a) M [2 + R3 + R4]
b) M [2 + (R3 × R4)]
c) M [2 × (R3 + R4)]
d) M [2 + M(R3) + M(R4)]
e) M [[R3] + [R4]] + 2

(1 mark)

Q3 ADD A in one address instruction format means

a) AC ← AC + A
b) AC ← AC + M [A]
c) REG ← AC + M [A]
d) REG ← REG + A
e) REG ← REG + M[A]

(1 mark)

Q4 Two main types of branch instructions are _____.

a) compare and jump
b) conditional branch and unconditional branch
c) jump and unconditional branch
d) logical branch and conditional branch
e) skip and conditional branch

(1 mark)

Q5 In which mode the operand is placed in one of 8-bit or 16-bit general purpose registers?

a) Immediate addressing
b) Implied addressing
c) Register Indirect
d) Register mode
e) Stack pointer mode

(1 mark)

Q6 In the following indexed addressing mode instruction, MOV R7, 8(LOC) the effective address is _____.

a) R7 = LOC
b) R7 = M[LOC]
c) R7 = LOC + 8
d) R7 = LOC × 8
e) R7 = M[LOC + 8]

(1 mark)

Q7 What is the postfix expression for the following infix expression?

a / b ^ c – d

a) abc^/d-
b) ab/cd^-
c) ab/^cd-
d) abcd^/-
e) abcd/^-

(1 mark)

Q8 What is the postfix expression for the corresponding infix expression?

a + b * c + (d * e)

a) abc+*de*+
b) abc*+de*+
c) abc*+(de)*+
d) ab*c+de+*
e) a+bc*de+*

(1 mark)

Q9 If a processor clock rated as 500 million cycles per second, then its' clock period is _____.

a) 2×10^{-3}
b) 2×10^{-6}
c) 2×10^{-8}
d) 2×10^{-9}
e) 2×10^{-10}

(1 mark)

Q10 The interrupt-request line is a/an _____ along which the device is allowed to send the interrupt signal.

a) address line
b) control line
c) data line
d) memory address line
e) None of the mentioned

(1 mark)

Q11 In memory mapped I/O _____.

a) a part of the memory is specifically set aside for the I/O operation
b) the I/O devices and the memory have an associated address space
c) the I/O devices and the memory share the same address space
d) the I/O devices have a same address space
e) the I/O devices have a separate address space

(1 mark)

Q12 The time between the receival of an interrupt and its' services is _____.

a) cycle time
b) interrupt delay
c) interrupt latency
d) propagation delay
e) switching time

(1 mark)

Q13 Which of the following groups consists of only input devices?

i) Mouse
ii) Keyboard
iii) Monitor
iv) Touchpad

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv
e) i, ii, iii and iv

(1 mark)

Q14 From amongst the following given scenarios determine the right one to justify interrupt mode of data transfer.

i) Bulk transfer of several kilobyte
ii) Keyboard inputs
iii) Moderately large data transfer of more than 1kb
iv) Short events like mouse action

a) i
b) ii
c) i and iv
d) i and iii
e) i, ii, and iv

(1 mark)

Q15 Which one of the following is **TRUE** about a CPU having a single interrupt request line and single interrupt grant line?

i) Multiple interrupting devices are possible
ii) Multiple interrupting devices are not possible
iii) Vectored interrupts are possible
iv) Vectored interrupts are not possible

a) i and iii
b) i and iv
c) ii and iii
d) ii and iv
e) None of the mentioned

(1 mark)

Q16 The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?

a) control signal
b) DMA
c) exception
d) interrupts
e) signal handling

(1 mark)

Q17 How can the processor ignore other interrupts when it is servicing one?

i) By disabling the devices from sending the interrupts.
ii) By increasing the number of program counter
iii) By turning off the interrupt request line.
iv) By using edge-triggered request line

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q18 Input and output devices are notified of a read or write operation by _____.

a) enabling the read or write bits of the devices
b) pending an extra bit of the address
c) raising an appropriate interrupt signal
d) sending a special signal along the BUS
e) sending a read or write bits of the devices

(1 mark)

Q19 Which of these busses is unidirectional?

i) Data bus
ii) Control bus
iii) Counter bus
iv) Address bus

a) i and ii
b) i and iii
c) ii and iii
d) ii and iv
e) iii and iv

(1 mark)

Q20 Which register holds instructions/data temporarily after it is brought to the processor from main memory?

a) General Purpose Register
b) Instruction Register
c) Memory Address Register
d) Memory Data Register
e) Program Counter

(1 mark)

Q21 What happens immediately after data is returned to the Memory Data Register (MDR) from Memory in the Fetch stage?

a) Data from the MDR is copied into the Memory Address Register
b) Data from the MDR is copied into the Instruction Register
c) Data from the MDR is copied into the Program Counter
d) Data from the MDR is sent back to memory along the data bus
e) Data from the MDR is sent to address register

(1 mark)

Q22 CPU performance can be affected by:

i) Cache size
ii) Clock speed
iii) Number of cores
iv) Number of instructions in a program

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q23 Which of these happen in the Fetch stage?

i) the Program Counter is incremented by one
ii) the value in the Program Counter is sent to memory on the address bus
iii) the value returned from memory is added to the value in the Memory Address Register
iv) the value returned from memory is stored in the current instruction register

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q24 Which of the following happen in the Execute stage?

i) Data from memory is copied into the Accumulator
ii) Data from memory and Accumulator are executed
iii) The Program Counter value is copied into the Memory Address Register
iv) Data from memory is added to the Accumulator, and the result is stored there

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q25 Which of the following does not happen in the Execute stage?

i) The ALU executes the instruction for the value in the Accumulator
ii) The control unit decodes the IR to determine the data value
iii) The data in the IR is added to the value in the Accumulator
iv) The data in the IR is copied into the Memory Address Register

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q26 LOAD X means:

a) Load the current Memory Address Register value to address X
b) Load the current Memory Data Register value with address value of X
c) Load the value from Memory Address Register with address value of X
d) Load the X value to Memory Address Register
e) Load the X value to Memory Data Register

(1 mark)

Q27 _____ show one of the processes happen in Fetch stage.

a) AC ← MDR + [AC]
b) IR ← PC
c) MAR ← PC
d) MDR ← PC
e) PC ← [PC] + Branch offset

(1 mark)

Q28 Cache memory acts between _____.

i) CPU
ii) RAM
iii) External Hard Disk
iv) Secondary Storage

a) i and ii
b) i and iii
c) ii and iii
d) ii and iv
e) iii and iv

(1 mark)

Q29 How many bytes does a memory can be contained if it has 1500 words of 256 bits each?

a) 384 Kbyte
b) 384000 Kbyte
c) 48 Kbyte
d) 4800 Kbyte
e) 48000 Kbyte

(1 mark)

Q30 Select the **TRUE** statements about ROM:

i) It is used for booting purposes
ii) It is used for arithmetic execution purposes
iii) It store the permanent information
iv) It do not lose memory when power is removed

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q31 Which statement best describes ROM?

a) A flash memory chip that contains a small amount of non-volatile memory
b) A memory store containing a large amount of volatile memory
c) A memory store containing a small amount of volatile memory
d) A memory which used to store data on a temporary basis
e) A register within the CPU responsible for storing memory addresses

(1 mark)

Q32 In comparison with static RAM memory, the dynamic RAM memory is _____.

i) higher in bit density
ii) faster
iii) expensive
iv) cheaper

a) i and iii
b) i and iv
c) ii and iii
d) ii and iii
e) None of the mentioned

(1 mark)

Q33 How many 64kB RAM chips are needed to provide a memory capacity of 16384KB?

a) 64
b) 128
c) 256
d) 512
e) 1024

(1 mark)

Q34 If a memory has 50 cache hits (requests) and 30 misses, the cache hit rate is _____.

a) 40.0%
b) 60.0%
c) 62.5%
d) 66.6%
e) 80.0%

(1 mark)

Q35 When is Virtual Memory needed or used by a computer?

i) When chosen by the user or computer administrator
ii) When multitasking is required
iii) When RAM becomes full because of too many programs running at once
iv) When users wish to store data on an external server such as cloud server
v) When users wish to use large programs

a) i, ii and iii
b) i, ii, and iv
c) ii, iii and iv
d) ii, iii, and v
e) iii, iv, and v

(1 mark)

Q36 Which of the following statements are **NOT CORRECT** about the main memory of a computer?

i) In main memory, data gets lost when power is switched off
ii) Main memory including both RAM and ROM
iii) Main memory is faster than registers
iv) Main memory is smaller than cache

a) i, ii and iii
b) i, ii and iv
c) i, iii, and iv
d) ii, iii and iv
e) i, ii, iii, and v

(1 mark)

Q37 A non-pipeline system takes 50ns to process a task. The same task can be processed in six-segment pipeline with a clock cycle of 10ns. By considering that there is no hazard happen in the system, determine approximately the speedup ratio of the pipeline for 500 tasks.

a) 4.95
b) 5
c) 5.5
d) 5.7
e) 6

(1 mark)

Q38 Which of the following are advantages of pipelining?

i) Faster ALU can be designed when pipelining is used
ii) Increase in the number of pipeline stages increases the number of instructions executed simultaneously.
iii) Instruction latency increases in pipelined processors.
iv) Pipelining increases the overall performance of the CPU

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q39 Hazard in pipeline including _____.

i) data hazard
ii) execution hazard
iii) instruction hazard
iv) structural hazard

a) i, ii and iii
b) i, ii, and iv
c) i, iii and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q40 To increase the speed of memory access in pipelining, we make use of _____.

a) buffers
b) cache
c) random access memory
d) special memory locations
e) special purpose registers

(1 mark)

Q41 If the processing speed goes from 500MHz to 2GHz, what effect does this have on performance?

a) The maximum number of instructions executed per second doubles
b) The maximum number of instructions executed per second halves
c) The maximum number of instructions executed per second octuplets
d) The maximum number of instructions executed per second quadruples
e) The maximum number of instructions executed per second quarters

(1 mark)

Q42 Which of the following is disadvantage of pipelining?

a) Cycle time of the processor is reduced
b) Increase the CPU performance
c) Increase the required memory
d) The design of pipelined processor is costly to manufacture
e) The instruction latency is less

(1 mark)

Q43 Which of the following statement is **TRUE** with respect to instruction pipeline with k stages?

i) Minimum speed up can be achieved with k staged pipeline is k
ii) Maximum speed up that a pipeline can provide is k theoretically
iii) With pipeline throughput of the system is increased
iv) When k increase, the total time will be increased

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(1 mark)

Q44 Which of the following statements is **TRUE**?

i) Write after Write (WAW) hazard can be mitigated by data forwarding
ii) Both WAW and WAR hazards can be mitigated by data forwarding
iii) Write after Read (WAR) hazard can be mitigated by data forwarding

a) i and ii
b) i and iii
c) ii and iii
d) i, ii and iii
e) None of the mentioned

(1 mark)

Q45 The situation where in the data of operands are not available is called _____.

a) control hazard
b) data hazard
c) execution hazard
d) instruction hazard
e) structural hazard

(1 mark)

Q46 Product support professionals repeatedly create complex application environments to debug problems reported by customers. How might provisioning in a cloud computing solution help the product support team's efficiency?

a) It allows the team to rapidly deploy complex application environments
b) It helps the team identify bugs in the code
c) It reduces the amount of computer hardware used by the team
d) It reduces the cost of computer hardware used by the team
e) It reduces the number of environments the team must recreate

(1 mark)

Q47 Which statement is **NOT TRUE** about a cloud computing environment?

i) It is invulnerable with data loss
ii) It enables users to access systems regardless of their location
iii) It introduces latency as the servers are geographically dispersed
iv) It can increase the capital expenses for hardware and software setting up

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv
e) None of the mentioned

(1 mark)

Q48 What are some of the cloud benefits that make it lower risk for enterprises to adopt cloud?

i) Data security associated with loss or unavailability of data causing business disruption
ii) Diversity of standard for technology integration lead to data leakage
iii) The pay-as-you-go model allows enterprises to experiment with technologies as opposed to making long-term decisions based on little or no trial
iv) The speed with which applications can be up and running on the cloud versus months on traditional platforms, means enterprises can experiment, fail fast, learn, and course correct without setting them back significantly

a) i and ii
b) i and iv
c) ii and iii
d) ii and iv
e) iii and iv

(1 mark)

Q49 Which are some of the key components of cloud infrastructure?

i) IaaS provide a static service
ii) IaaS providers install required applications on the physical machines
iii) IaaS providers manage large data centres and the service is highly scalable
iv) IaaS providers can manage both small and large companies

a) i and ii
b) i and iii
c) ii and iii
d) ii and iv
e) iii and iv

(1 mark)

Q50 A company that originally planned its web-based IT system to support 10,000 users suddenly notices that there is four times increase in demand. If the company has deployed its system in a true cloud environment, what are the incremental maintenance costs to adding new resources to this environment?

a) Twice its original costs of deployment
b) Three times its original costs of deployment
c) Four times its original costs of deployment
d) Eight times its original costs of deployment
e) Negligible

(1 mark)

SECTION B: SUBJECTIVE QUESTIONS (50 MARKS)

Q51 (a) Explain the different between Memory Address Register (MAR) and Memory Data Register (MDR).

(2 marks)

(b) Explain the steps required in instruction execution cycle.

(2 marks)

Q52 Consider the List of Opcode is as in **Table Q52** and content in Memory Address Register (MAR) in **Figure Q52**.

Table Q52: List of Opcode

0000 = Halt
0001 = Load AC from Memory
0010 = Store AC to Memory
0011 = Multiply to AC from Memory
0100 = Subtract to AC from Memory
0101 = Add to AC from Memory

MAR	MDR
601	5
602	2
603	17
604	4
605	0

Figure Q52: The content in Memory Address Register (MAR)

(a) Writes the MDR program fragment in **Figure Q52(a)** from M[301] till M[308] (the bold box) by considering its' respective Register Transfer Notation (RTN) code. MDR Program fragment for M[300] is provided as an example.

MAR	MDR	RTN
300	1601	AC ← M[601]
301		AC ← AC * M[602]
302		M[700] ← AC
303		AC ← M[603]
304		AC ← AC – M[604]
305		M[701] ← AC
306		AC ← M[700]
307		AC ← AC + M[701]
308		M[702] ← AC

Figure Q52(a): Program fragment code associate with MAR and its' respective Register Transfer Notation (RTN) code

Note:
Write your answer in bold box in the **Figure Q52(a).**

(8 marks)

(b) Based on the execution done in **Q52(a)** calculate the final value for M[700], M[701] and M[702].

(3 marks)

Q53 Illustrate the memory hierarchy. Explain its characteristic in terms of its size, speed and price.

(3 marks)

Q54 (a) Consider a 4GB Main Memory system with hit time access of 1.5cc, hit rate of 99.8% and miss penalty of 1000cc. Calculate the Average Memory Access Time (AMAT) for this memory.

(3 marks)

(b) Assume that the Main Memory in **Q54(a)** is assist by 8Mbyte L2 Cache and 16Kbyte L1 Cache. By considering the parameter given in **Table Q54(b)** and AMAT obtained in **Q54(a)**, calculate the AMAT for the whole system.

Memory Type	Parameter	Value
L1 cache 16Kbyte	Hit rate	97 %
	Hit time	1.7cc
L2 cache 8Mbyte	Hit rate	96%
	Hit time	15cc

(6 marks)

(c) Calculate the global miss rate for the whole system.

(2 marks)

Q55 Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Given CPU A has a set of instructions to run as shown in **Listing Q55**. The instruction format for instructions in **Listing Q55** is shown in **Figure Q55**.

```
MOV R7, #4;
MOV R8, #5;
MOV R7, #6;
MUL R8, R7;
```

Listing Q55

Operation	Destination Operand	Source operand

Figure Q55

The execution of each instruction involves five steps (Fetch Instruction, Decode, Read Operand, Execute and Write Result).

Assume that this pipeline system uses:
1 cycle to perform Fetch Instruction (FI),
1 cycle to perform Decode (D),
2 cycles to Read Operand (RO),
2 cycles to perform Execution (E),
1 cycle to perform Write Result (WR).

(a) Write the final value in register R8 at the end of **Listing Q55** instructions.

(2 marks)

(b) Illustrate the execution of instructions in **Listing Q55** if the CPU A implements no-pipelined method.

(3 marks)

(c) Illustrate the execution of instructions in **Listing Q55** if CPU A implements pipeline method.

(3 marks)

(d) Compare the Cycle per Instruction (CPI) for both non-pipelined and pipeline method. Calculate the speedup factor for this system.

(2 marks)

(e) Instructions in **Listing Q55** has been simulated in CPU simulator, however the result in register R8 given by the simulator is 20, different with the prediction value. By using your answer in **Q55(c)**, explain this situation by relating with hazard that may happen in pipeline method.

(3 marks)

(f) Suggest modification that should be done to the **Listing Q55** so that the result in register R8 is correct.

(2 marks)

Q56 Identify **TWO (2)** Cloud providers that are commonly used by the user.

(2 marks)

Q57 Security is among the top concerns with cloud computing. Explain **FOUR (4)** cloud computing security risks.

(4 marks)

- **END OF QUESTIONS –**