Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2022/2023

COURSE NAME	:	VLSI SYSTEM
COURSE CODE	:	BEJ 43103
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	FEBRUARY 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER ALL QUESTIONS
		2.THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.**
		3.STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) For this function,

$$F = \overline{A + E(B + CD)},$$

(i) Design a fully complementary static CMOS circuit using minimum number of transistors to realize the logic function.

(8 marks)

(ii) Draw the consistent Euler path for the circuit.

(3 marks)

(iii) Draw the most compact stick diagram representing the circuit given by the equation. Clearly label the stick diagram.

(8 marks)

(b) Identify and suggest a method to prevent the contention problem by illustrating the method for Boolean equation, $Y = \overline{\left(\overline{A(B + C)}.E\right) + D}$

(6 marks)

Q2 (a) Given a CMOS circuit in **Figure Q2(a)**,

(i) Analyze the CMOS logic circuit and determine the Boolean expression for output X.

(4 marks)

(ii) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability on an inverter. Given that the minimum transistor length (L) is 2λ and the width (W) is 3λ; and the mobility of the electron is 2 times of the hole's mobility.

(8 marks)

(iii) Calculate the total driving strength for inverter and minimal parasitic delay for the circuit.

(6 marks)

(b) (i) List **THREE (3)** sources of leakage current in CMOS transistor.

(3 marks)

(ii) Describe the reason why leakage current increases with the advancement of technology scaling in CMOS transistor.

(4 marks)

Q3 (a) **Figure Q3(a)** shows a dynamic decoder circuit.

(i) Analyse the circuit and construct a truth table to show the relationship between the input (A1 and A0), and the output (D0 to D3).

(4 marks)

(ii) Determine the equations for all the output D_3, D_2, D_1 and D_0.

(8 marks)

(iii) Describe the operation of the circuit during the evaluation mode when A1 = 1 and A0 = 0 i.e. by evaluating which transistors are ON and OFF. Determine the value of all the output at this state.

(8 marks)

(b) A full adder accepts two input bits (A, B) and an input carry (C_{in}) and generates a sum output, $Sum = A \oplus B \oplus C$ and an output carry, $C_{out} = AB + C_{in}(A + B)$. Design the full adder at transistor level with minimum number of transistors using pseudo-nMOS method by showing the circuit for C_{out}. Clearly label the designed circuit. Assume all the inverted form of the inputs are available.

(5 marks)

Q4 (a) D flip-flop can be built by using SR clocked NAND based as shown in **Figure Q4(a)**.

(i) Draw a gate level for the D flip-flop using SR clocked NAND based.

(2 marks)

(ii) Determine the Boolean equation of output, Q and $\bar{Q}$

(5 marks)

(iii) Design the D flip-flop using minimum static CMOS using Boolean equation in **Q4(a)(ii)**.

(8 marks)

(b) Generate a complete test set that comprises a minimum number of tests by using path sensitization in the circuit in **Figure Q4(b)**.

(10 marks)

- END OF QUESTIONS –

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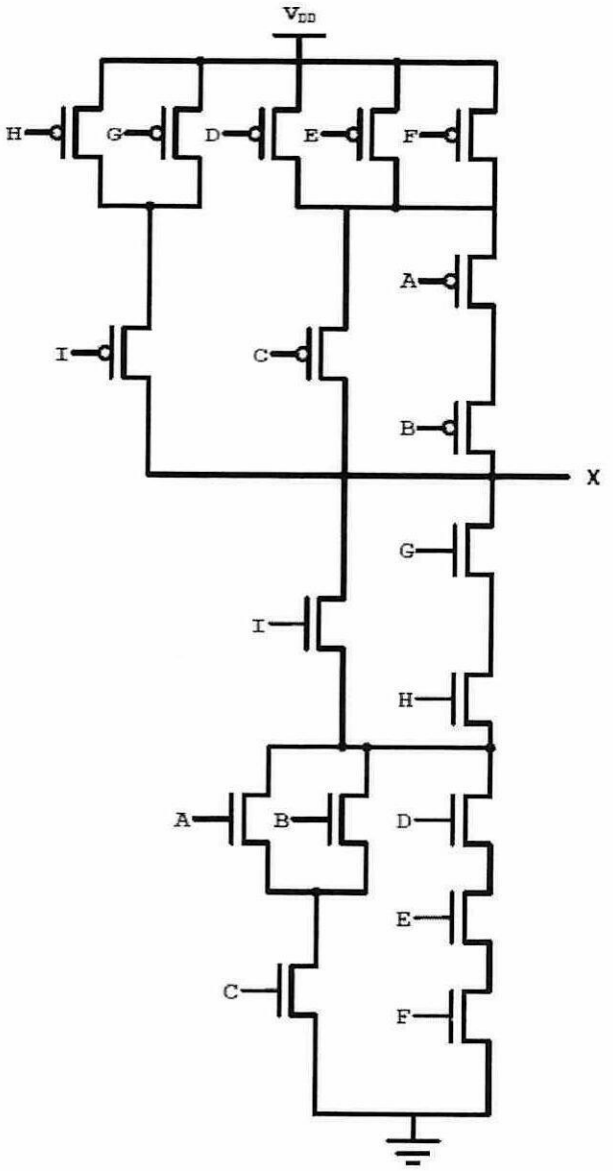

Figure Q2(a)

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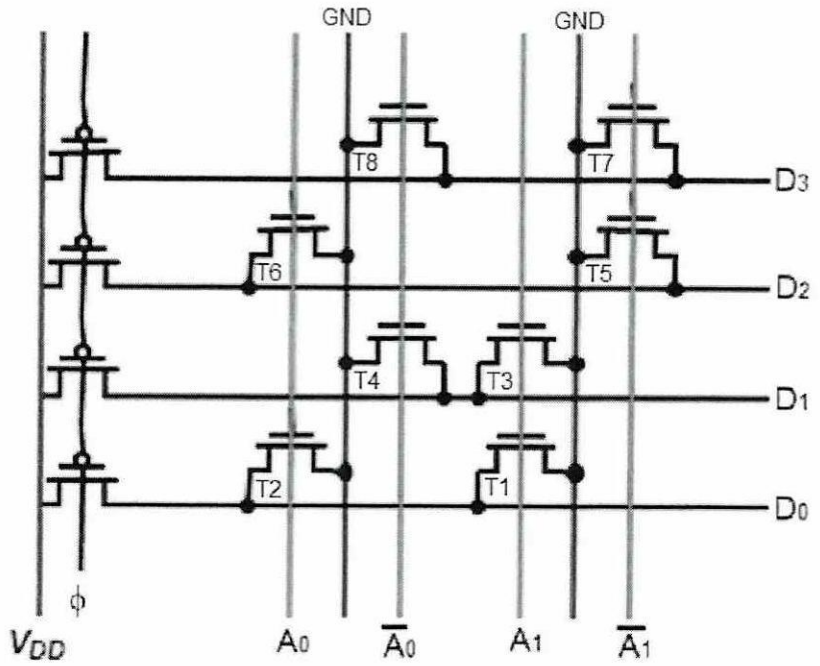

Figure Q3(a)

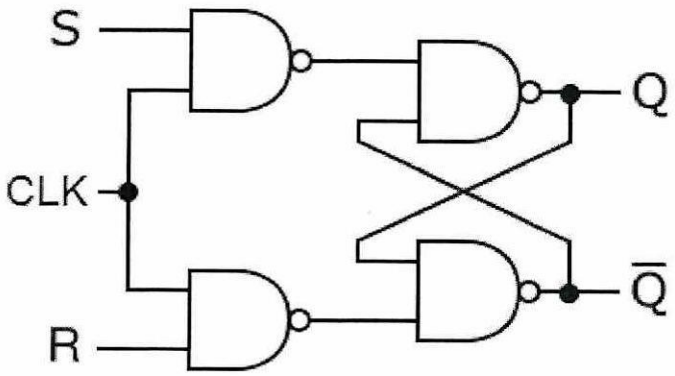

Figure Q4(a)

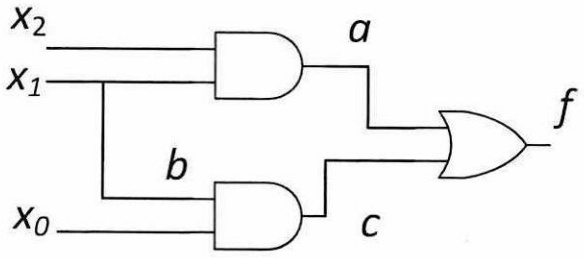

Figure Q4(b)