Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2022/2023

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEJ 30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	FEBRUARY 2023
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS IN **SECTION A IN OMR SHEET** AND ALL QUESTIONS IN **SECTION B IN THE QUESTION BOOKLET** 2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK.** 3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **FIFTEEN (15)** PAGES

SECTION A: OBJECTIVE QUESTIONS (50 MARKS)

Q1 In which mode the operand is placed in one of 8-bit or 16-bit general purpose registers?

a) Register mode
b) Register Indirect
c) Implied addressing
d) Immediate addressing

(1 mark)

Q2 What is the postfix expression for the corresponding infix expression?

a + b * c + (d * e)

a) abc*+de*+
b) abc+*de*+
c) a+bc*de+*
d) abc*+(de)*+

(1 mark)

Q3 In the following indexed addressing mode instruction, MOV R1, 2(LOC) the effective address is _____.

a) R1 = LOC
b) R1 = M[LOC]
c) R1 = LOC + 2
d) R1 = M[LOC+2]

(1 mark)

Q4 What is the effective address for ADD 5(R1, R2)

a) M [5+R1+R2]
b) M [5+(R1*R2)]
c) M [5+m(R1)+m(R2)]
d) M [[R1]+[R2]]+5

(1 mark)

Q5 ADD D in one address instruction format means

a) AC ← AC + D
b) AC ← AC + M [D]
c) REG ← REG + D
d) REG ← REG + M[D]

(1 mark)

Q6 Which register is used to store the value of arithmetic and logical operation?

a) Controlled
b) Accumulator
c) Logical register
d) Arithmetic register

(1 mark)

Q7 Two main types of branch instructions are/is _____.
a) conditional branch
b) unconditional branch
c) logical branch and conditional branch
d) conditional branch and unconditional branch

(1 mark)

Q8 If a processor clock rated as 2500 million cycles per second, then its' clock period is _____.
a) 4×10^{-10}
b) 4×10^{-9}
c) 4×10^{-6}
d) 4×10^{-3}

(1 mark)

Q9 What is the postfix expression for the following infix expression?

a / b ^ c – d

a) abc^/d-
b) ab/cd^-
c) ab/^cd-
d) abcd^/-

(1 mark)

Q10 The interrupt-request line is a/an_____ along which the device is allowed to send the interrupt signal.
a) data line
b) control line
c) address line
d) None of the mentioned

(1 mark)

Q11 In memory mapped I/O _____.
a) the I/O devices have a separate address space
b) the I/O devices and the memory share the same address space
c) the memory and I/O devices have an associated address space
d) a part of the memory is specifically set aside for the I/O operation

(1 mark)

Q12 Input and output devices are notified of a read or write operation by _____.
a) pending an extra bit of the address
b) raising an appropriate interrupt signal
c) sending a special signal along the BUS
d) enabling the read or write bits of the devices

(1 mark)

Q13 The time between the receival of an interrupt and its' services is _____.
a) cycle time
b) interrupt delay
c) switching time
d) interrupt latency

(1 mark)

Q14 The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?

a) DMA
b) exception
c) interrupts
d) signal handling

(1 mark)

Q15 Which of the following groups consists of only input devices?

i) Mouse
ii) Keyboard
iii) Monitor
iv) Touchpad

a) i, ii, and iii
b) i, ii, and iv
c) ii, iii, and iv
d) i, ii, iii and iv

(1 mark)

Q16 From amongst the following given scenarios determine the right one to justify interrupt mode of data transfer.

i) Keyboard inputs
ii) Short events like mouse action
iii) Bulk transfer of several kilobyte
iv) Moderately large data transfer of more than 1kb

a) i
b) iv
c) i and ii
d) i,ii, and iv

(1 mark)

Q17 How can the processor ignore other interrupts when it is servicing one?

i) By using edge-triggered request line
ii) By turning off the interrupt request line.
iii) By disabling the devices from sending the interrupts.

a) i and ii
b) i and iii
c) ii and iii
d) i, ii, and iii

(1 mark)

Q18 Which of the following is/are true about a CPU having a single interrupt request line and single interrupt grant line?

i) Neither vectored nor multiple interrupting devices is possible.
ii) Vectored interrupts are not possible but multiple interrupting devices are possible.
iii) Vectored interrupts are possible and multiple interrupting devices are not possible.
iv) Both vectored and multiple interrupting devices are possible.

a) iii
b) iv
c) i and iv
d) iii and iv

(1 mark)

Q19 Which of these does not happen in the Fetch stage?

a) the Program Counter is incremented by 1
b) the value in the Program Counter is sent to memory on the address bus
c) the value returned from memory is added to the value in the accumulator.
d) the value returned from memory on the data bus is stored in the current instruction register

(1 mark)

Q20 _____ show one of the process happen in Fetch stage.

a) MAR ← PC
b) IR ← MDR
c) AC ← MDR + [AC]
d) MDR ← PC

(1 mark)

Q21 LOAD X means

a) Load the X value
b) Load the current Memory Data Register value
c) Load the value from Memory Address Register with address value of X
d) Memory updates the data at the given address using the value supplied on the data bus

(1 mark)

Q22 What happens immediately after data is returned to the Memory Data Register (MDR) from Memory in the Fetch stage?

a) Data from the MDR is copied into the Accumulator
b) Data from the MDR is copied into the Program Counter
c) Data from the MDR is sent back to memory along the data bus
d) Data from the MDR is copied into the Instruction Register

(1 mark)

Q23 What happens in the Execute stage?

a) The ALU executes the instruction for the value in the Accumulator
b) The data in the IR is added to the value in the Accumulator
c) The control unit decodes the IR to determine the data value
d) The data in the IR is copied into the Memory Address Register

(1 mark)

Q24 Which of these is NOT something that can happen in the Execute stage?

a) Data from Memory is copied into the Accumulator
b) Data from Memory and Accumulator are executed
c) The Program Counter value is copied into the Memory Address Register
d) Data from Memory is added to the Accumulator, and the result is stored in the Accumulator

(1 mark)

Q25 Which of these busses is unidirectional?

i) Data bus
ii) Control bus
iii) Counter bus
iv) Address bus

a) i and ii
b) i and iii
c) ii and iv
d) iii and iv

(1 mark)

Q26 Which of these does **not** affect CPU performance?

a) Cache Size
b) Clock Speed
c) Number of Cores
d) Number of instructions in a program

(1 mark)

Q27 Which register holds instructions/data temporarily after it is brought to the processor from main memory?

a) Program Counter
b) Instruction Register
c) General Purpose Register
d) Memory Address Register

(1 mark)

Q28 How many bytes does a memory can be contained if it has 1500 words of 256 bits each?

a) 48 Kbyte
b) 48000 Kbyte
c) 384 Kbyte
d) 384000 Kbyte

(1 mark)

Q29 How many 64kB RAM chips are needed to provide a memory capacity of 512kB?

a) 8
b) 64
c) 128
d) 256

(1 mark)

Q30 The memory devices which are like EEPROM but differ in the cost effectiveness is _____.

a) CMOS
b) Flash memory
c) Memory sticks
d) Blue-ray devices

(1 mark)

Q31 Cache memory acts between _____.

a) CPU and RAM
b) RAM and ROM
c) CPU and Hard Disk
d) Primary Storage and Secondary Storage

(1 mark)

Q32 If a memory has 43 cache hit and 11 cache miss, the hit rate is _____

a) 26%
b) 43%
c) 75%
d) 80%

(1 mark)

Q33 Which statement best describes ROM?

a) A memory store containing a large amount of volatile memory
b) A memory store containing a small amount of volatile memory
c) A register within the CPU responsible for storing memory addresses
d) A flash memory chip that contains a small amount of non-volatile memory

(1 mark)

Q34 In comparison with static RAM memory, the dynamic RAM memory has _____.

a) lower bit density and lower power consumption
b) lower bit density and higher power consumption
c) higher bit density and lower power consumption
d) None of the mentioned

(1 mark)

Q35 When is Virtual Memory needed or used by a computer?

a) When chosen by the user or computer administrator
b) When ROM is too small and struggles to store the Operating System
c) When users wish to store data on an external server such as cloud server
d) When RAM becomes full because of too many programs running at once

(1 mark)

Q36 Disadvantage of dynamic RAM over static RAM is _____.

a) variable speed
b) lower packing density
c) higher power consumption
d) need to refresh the capacitor charge every once in two milliseconds

(1 mark)

Q37 If the processing speed goes from 1GHz to 4GHz, what effect does this have on performance?

a) The maximum number of instructions executed per second halves
b) The maximum number of instructions executed per second doubles
c) The maximum number of instructions executed per second quarters
d) The maximum number of instructions executed per second quadruples

(1 mark)

Q38 Which of the following is/are advantage of pipelining?

i) Instruction throughput increases.
ii) Faster ALU can be designed when pipelining is used.
iii) Pipelining increases the overall performance of the CPU.

a) i and ii
b) i and iii
c) ii and iii
d) i, ii, and iii

(1 mark)

Q39 Hazard in pipeline are as follows except _____.

a) data hazard
b) execution hazard
c) instruction hazard
d) structural hazard

(1 mark)

Q40 The situation where in the data of operands are not available is called _____.

a) stock
b) deadlock
c) data hazard
d) structural hazard

(1 mark)

Q41 If a unit completes its task before the allotted period, then _____.

a) it'll remain idle for the remaining time
b) its time gets reallocated to different task
c) it'll perform some other tasks in the remaining time
d) None of the mentioned

(1 mark)

Q42 To increase the speed of memory access in pipelining, we make use of _____.

a) cache
b) buffers
c) special purpose registers
d) special memory locations

(1 mark)

Q43 Which of the following is disadvantage of pipelining?

a) The instruction latency is less
b) Increase the CPU performance
c) Cycle time of the processor is reduced.
d) The design of pipelined processor is costly to manufacture.

(1 mark)

Q44 The average number of steps taken to execute the set of instructions can be made to be less than one by implementing _____ operation.

a) ISA
b) RISC
c) superscalar
d) non-pipeline

(1 mark)

Q45 If some combination of instructions cannot be accommodated because of resource conflicts, the processor is said to have a _____.

a) stall
b) data hazard
c) pipeline hazard
d) structural hazard

(1 mark)

Q46 Internet of Things will digitize the world by connecting:

i) Data
ii) People
iii) Process
iv) Search

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv

(1 mark)

Q47 Characteristics of a Smart Object including:

i) Actuator
ii) Power Source
iii) Sensors
iv) Tiny Low-Cost Computer

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q48 With the use of Internet of Things,

i) a manufacturer cannot repair more than 3 faults at one go.
ii) a manufacturer can set up an appointment to repair the fault.
iii) a manufacturer can integrate the data coming from various devices.
iv) a manufacturer can order the required parts to be used to make the repairs.

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q49 Which of the following fields is NOT the application in Internet of Things?

i) Daily Life
ii) Health and Security
iii) Traffic Monitoring
iv) Transport and Logistics

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) None of the mentioned

(1 mark)

Q50 The IoT reference model published by the IoT World Forum including the following levels:

i) Application
ii) Connectivity
iii) Data Accumulation
iv) Edge Computing

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

SECTION B: SUBJECTIVE QUESTIONS (50 MARKS)

Q51 (a) Describe the steps that CPU continuously carries in a cycle when processing a program.

(1 mark)

(b) Explain what is held in Memory Address Register (MAR)?

(1 mark)

(c) Justifies the purpose of Instruction Register (IR)?

(2 marks)

Q52 Consider the List of Opcode is as in **Table Q52** and Program Fragment is as in **Figure Q52**.

Table Q52: List of Opcode

0000 = Halt
0001 = Load AC from Memory
0010 = Store AC to Memory
0011 = Multiply to AC from Memory
0100 = Subtract to AC from Memory
0101 = Add to AC from Memory

MAR	MDR
200	1800
201	3801
202	2900
203	1802
204	4804
205	2901
206	1803
207	5902
208	2902

800	2
801	4
802	5
803	10
804	1

900	0
901	0
902	0

Figure Q52: Program fragment

(a) Writes the Register Transfer Notation (RTN) for program fragment from M[200] till M[208]. See **Figure Q52(a)** for example RTN notation for M[200].

MAR	MDR		Register Transfer Notation (RTN)
200	1800	⟶	AC ← M [800]
201	3801		
202	2900		
203	1802		
204	4804		
205	2901		
206	1803		
207	5902		
208	2902		

Figure Q52(a): Example RTN notation for M[200].

(8 marks)

(b) Identify the final value at M[900], M[901] and M[902].

(3 marks)

Q53 Identifies what is non-volatile memory and why it is required?

(2 marks)

Q54 Consider an XYZ microprocessor with 16 Kbyte L1 cache. The miss rate for this cache is 3% and the hit time is 2 cc. That microprocessor also has an 8 Mbyte, on-chip L2 cache. 95% of the time, data request to L2 cache are found and its hit time is 14 cc. If data is not found in L2 cache, a request is made to a 4Gbyte main memory. The miss penalty at main memory is 1000cc and its hit time is 1.5cc. On average, the memory access time for the main memory is 3.5cc.

(a) Explain what is the cache memory and its' purpose.

(2 marks)

(b) Calculate the percentage of data found in main memory (hit rate).

Memory Type	Parameter	Value
L1 cache 16Kbyte	Miss rate	3 %
	Hit time	2cc
L2 cache 8Mbyte	Hit rate	95%
	Hit time	14cc
Main Memory 4GB	Miss penalty	1000cc
	AMAT	3.5 cc
	Hit time	1.5 cc

(4 marks)

(c) Calculate the average memory access time for this system.

(4 marks)

Q55 Consider a 4096 block of Main Memory with number cache block is 128, where the size each cache block is 16 words. Calculate the number of tag, block and word, if the Direct Mapping Function is used.

(3 marks)

Q56 One way to improve the performance of a CPU is by arranging the hardware such that more than one operation can be performed at the same time. Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction takes place in a pipelined processor. Given CPU M has a set of instructions to run as shown in **Listing Q56**. The instruction format for instructions in **Listing Q56** is shown in **Figure Q56**. The execution of each instruction involves five steps (Fetch Instruction, Decode, Read Operand, Execute and Write Result). For each step, the execution time is 1 cycle.

```
MOV R01, #5;
MOV R02, #4;
MOV R01, #3;
MUL R01, R02;
```

Listing Q56

Operation	Destination Operand	Source operand

Figure Q56

(a) Write the final value in register R01 at the end of **Listing Q56** instructions.

(2 marks)

(b) Illustrate the execution of instructions in **Listing Q56** if the CPU M implements no-pipelined method.

(3 marks)

(c) Illustrate the execution of instructions in **Listing Q56** if the CPU M implements pipeline method.

(3 marks)

(d) Compare the Cycle per Instruction (CPI) for both non-pipelined and pipeline method. Calculate the speedup factor for these systems.

(2 marks)

(e) Instructions in **Listing Q56** has been simulated in CPU simulator, however the result in register R01 given by the simulator is 15, different with the prediction value. By using your answer in **Q56(c)**, explain this situation by relating with hazard that may happen in pipeline method.

(3 marks)

(f) Suggest modification that should be done to the **Listing Q56** so that the result in register R01 is correct.

(2 marks)

Q57 Identify five challenges or risk associated with IoT.

(5 marks)

- **END OF QUESTIONS –**