



UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER I
SESSION 2022/2023**

COURSE NAME : COMPUTER SYSTEMS ENGINEERING
COURSE CODE : BEJ42403 / BEC41603
PROGRAMME CODE : BEJ
EXAMINATION DATE : FEBRUARY 2023
DURATION : 3 HOURS
INSTRUCTION : 1. ANSWER ALL QUESTIONS
2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK**.
3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF FIVE (5) PAGES

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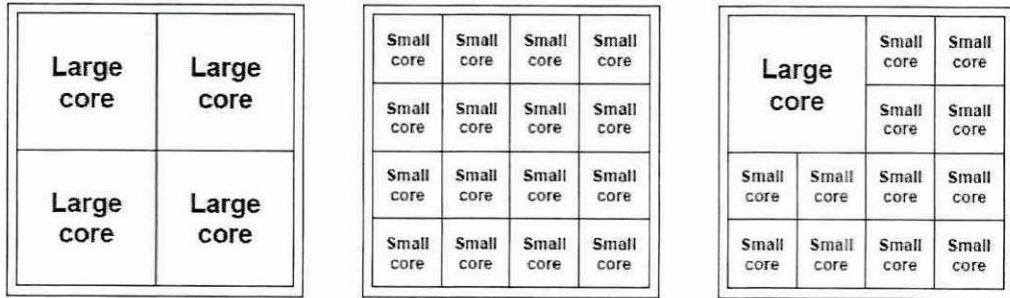
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Q1 (a) ALU is important element inside computer system.

(i) State the primary function of ALU. (2 marks)

(ii) Describe the superscalar with out of order issue (2 marks)

(b) Based on the information given at **Figure Q1(b)**, answer the following question:



	Large core	Small core
Microarchitecture	Out-of-order, 128-256 entry ROB	In-order
Width	3-4	1
Pipeline depth	20-30	5
Normalized performance	5-8x	1x
Normalized power	20-50x	1x
Normalized energy/instruction	4-6x	1x

Figure Q1(b)

(i) analyze the architecture (showing the calculation process) that produce higher throughput. Assume that the serial performance for large and small core is 2 and 1 respectively. (3 marks)

(ii) analyze the architecture (showing the calculation process) that give better performance in term of power and energy consumption (3 marks)

(c) Based on **Q1(b)**, which architecture considered as the best architecture. Justify your answer. (2 marks)

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- Q2** (a) Describe the benefit of NUMA compare to UMA (1 marks)
- (b) By inserting the cache between the processor and main memory, demonstrate how the cache can reduce the execution time and energy consumption for an application. (2 marks)
- (c) Sketch two level catch between processor and main memory by labelling the size of the cache at each level. (3 marks)
- (d) Analyse which structure is belongs to **Figure Q2(d)** by giving the justification. (5 marks)

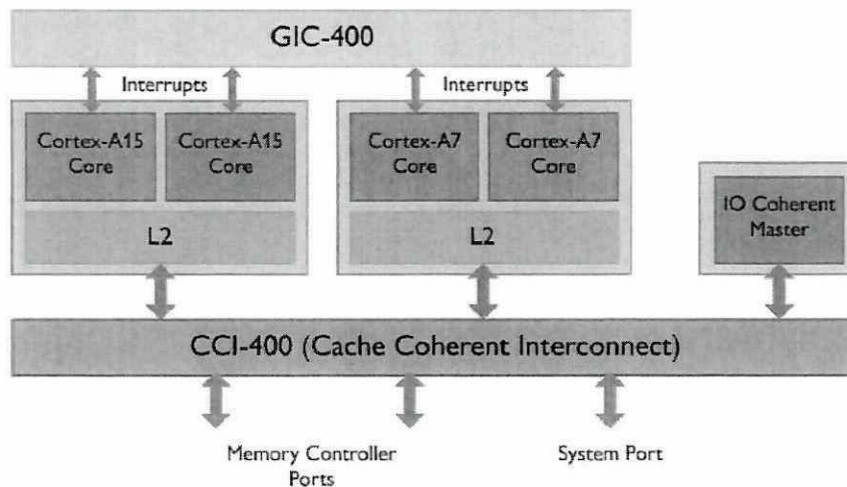


Figure Q2(d)

- Q3** (a) Based on the formula of Amdahl's law, where

$$S(N) = \frac{1}{(1 - P) + \frac{P}{N}}$$

implement the new formula if the number of processor, N is infinity. Justify your answer.

- (b) Based on **Figure Q3(b)**, prove that the speedup equal to 10 if the number of processor equal to 8192 with the parallel portion equal to 90%. (3 marks)

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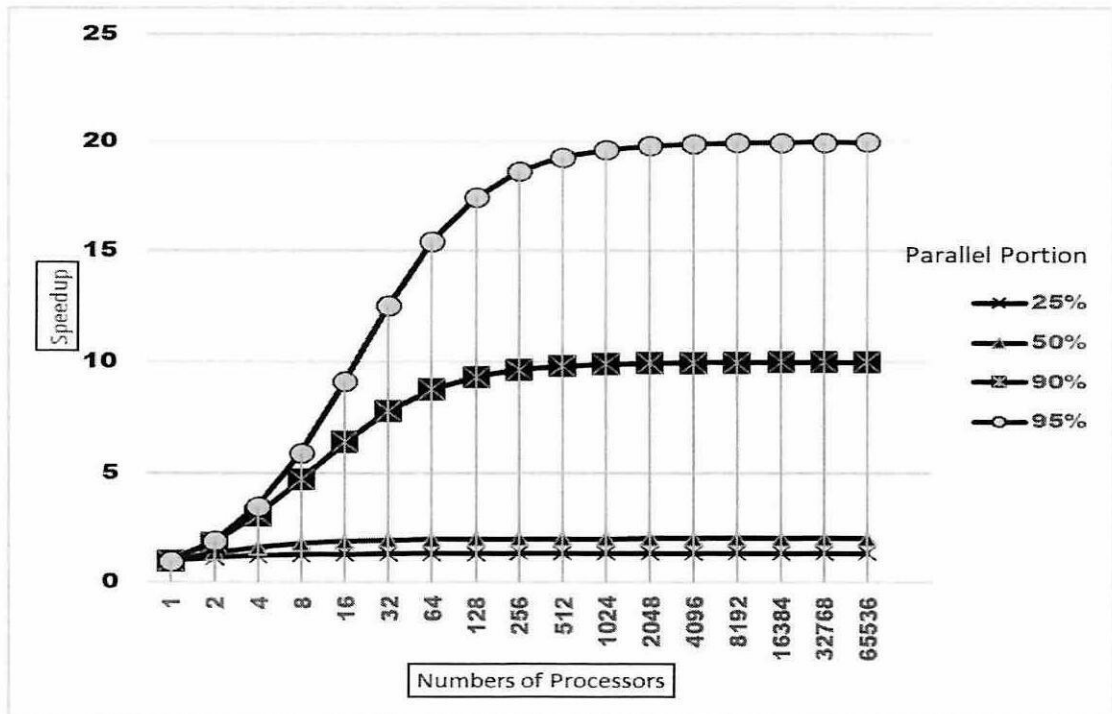


Figure Q3(b)

(3 marks)

- (c) Analyse the code as shown at Listing Q3(c) by giving the explanation from line 7 until line 16.

```

Line 1  #include <stdio.h>
Line 2  #include <omp.h>
Line 3  int main()
Line 4  {
Line 5    int rank;
Line 6    int a;

Line 7    #pragma omp parallel
Line 8    private(a,rank)
Line 9    {
Line 10     a=50000;
Line 11     #pragma omp master
Line 12     {
Line 13     a= -50000;
Line 14     }
Line 15     rank = omp_get_thread_num();
Line 16     printf("Rank:%d; A= %d\n", rank,a);

Line 17  }
Line 18  return 0;
Line 19  }
    
```

Listing Q3(c)

(4 marks)

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- (d) Produce the possible output if the number of thread used is 7. (3 marks)
- Q4** (a) State the purpose of synchronization. (3 marks)
- (b) Explain the important of critical section. (2 marks)
- Q5** (a) Differentiate between CPU and GPU. (2 marks)
- (b) Based on **Listing Q5(b)**, examine the portions of the code that are executed in parallel and serial.

```

__global__ void add(int *a, int *b, int *c)
{
    *c = *a + *b;
}
int main(void)
{
    int a, b, c; // host copies of a, b, c
    int *d_a, *d_b, *d_c; // device copies of a, b, c
    int size = sizeof(int);

    cudaMalloc((void **)&d_a, size);
    cudaMalloc((void **)&d_b, size);
    cudaMalloc((void **)&d_c, size);

    a = 2; b = 7;

    cudaMemcpy(d_a, &a, size, cudaMemcpyHostToDevice);
    cudaMemcpy(d_b, &b, size, cudaMemcpyHostToDevice);

    add<<<1,1>>>(d_a, d_b, d_c);

    cudaMemcpy(&c, d_c, size, cudaMemcpyDeviceToHost);

    cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);

    return 0;
}

```

Listing Q5(b)

- (5 marks)
- (c) Explain the important of HPC cloud (2 marks)

-END OF QUESTIONS -