Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2022/2023

COURSE NAME	:	ELECTRONICS
COURSE CODE	:	DAE 21303
PROGRAMME CODE	:	DAE
EXAMINATION DATE	:	FEBRUARY 2023
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWERS **ALL** QUESTIONS.
		2. THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK**.
		3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK.

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

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Q1 (a) In your own words, define briefly:

(i) Extrinsic semiconductor.

(2 marks)

(ii) Forward bias and reverse bias.

(2 marks)

(iii) Depletion region.

(2 marks)

(b) A centre-tapped full wave rectifier with a load, R_L is driven by a transformer with N_{pri} : N_{sec} turn ratio. The primary transformer is connected to a 120 V_{rms}, 50 Hz. The average voltage, V_{dc} that is produced by this rectifier is 27 V. Assuming diodes are ideal.

(i) Draw the schematic diagram of the circuit.

(2 marks)

(ii) Determine the transformer turns ratio.

(4 marks)

(ii) Sketch and label with values the input voltage, V_{in} and output voltage, V_o waveform of the rectifier.

(4 marks)

(iii) Calculate the Peak Inverse Voltage, PIV of each diode in the circuit.

(2 marks)

(c) Based on question **Q1(b)**, a 1.0 mF capacitor filter is now connected to the output of the rectifier circuit. If the dc current through the load is 0.1 A,

(i) Determine the filtered output ripple voltage, $V_{r(p-p)}$ and the average voltage, $V_{r(dc)}$.

(4 marks)

(ii) Sketch and clearly label the output ripple voltage from the filter.

(3 marks)

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Q2 (a) A voltage regulator circuit in **Figure Q2(a)** will maintain an output voltage of 20 V across a 1 kΩ load, R_L with an input, V_S varies between 30 V and 50 V. Determine:

(i) The minimum, I_{ZMin} and the maximum zener current, I_{ZMax} for the network if $R_{in} = 100\ \Omega$.

(10 marks)

(ii) The zener power rating, P_{zmin} and P_{zmax}.

(2 marks)

(b) The applications of the diode are shown in **Figure Q2(b)** with two different types of network.

(i) Determine the output voltage, V_o.

(8 marks)

(ii) Draw the waveform for each network.

(5 marks)

Q3 (a) **Figure Q3(a)(i)** depicts the load line and device characteristics of a fixed-bias network of Calculate the following based on the **Figure Q3(a)(ii)**.

(i) The common collector voltage, V_{CC}

(2 marks)

(ii) The base resistor, R_B

(2 marks)

(iii) The collector resistor, R_C

(2 marks)

(b) Determine the dc bias characteristics for the voltage-divider configuration of **Figure Q3(b)**.

(i) The dc base current, I_B

(6 marks)

(ii) The dc collector current, I_C

(1 mark)

(iii) The dc bias voltage, V_{CE}

(2 marks)

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(c) Refer to the amplifier network in **Figure Q3 (c)**.

(i) Sketch the ac equivalent circuit using r_e model.

(4 marks)

(ii) Determine the ac dynamic resistance, r_e if the dc base current, $I_B = 34.51\mu A$.

(2 marks)

(iii) Calculate the input impedance, Z_i and the output impedance, Z_o.

(4 marks)

Q4 (a) Determine the pinch-off voltage, V_P for a specific JFET if the drain current, $I_D = 4mA$ when the gate to source, $V_{GS} = -3V$ and the maximum drain current, $I_{DSS} = 12$ mA.

(3 marks)

(b) For the self-bias configuration of **Figure Q4(b)**, solve the following if given Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2$$

(i) The *quiescent*, Q-points (drain current, I_{DQ} and gate to source voltage, V_{GSQ}) by using graphical approach method.

(8 marks)

(ii) The drain to source voltage, V_{DS}, drain voltage, V_D, gate voltage, V_G and gate to source voltage, V_{GS}.

(7 marks)

(c) The fixed-bias configuration of **Figure Q4(c)** had an operating point defined by the gate to source voltage, $V_{GSQ} = -2.5$ V with the maximum drain current, $I_{DSS} = 10$ mA, the pinch-off voltage, $V_P = -4$ V, and the drain resistance, $r_d = 20$ kΩ. Determine:

(i) The input impedance Z_i.

(1 mark)

(ii) The output impedance Z_o.

(2 marks)

(iii) The voltage gain A_v.

(4 marks)

-END OF QUESTIONS –

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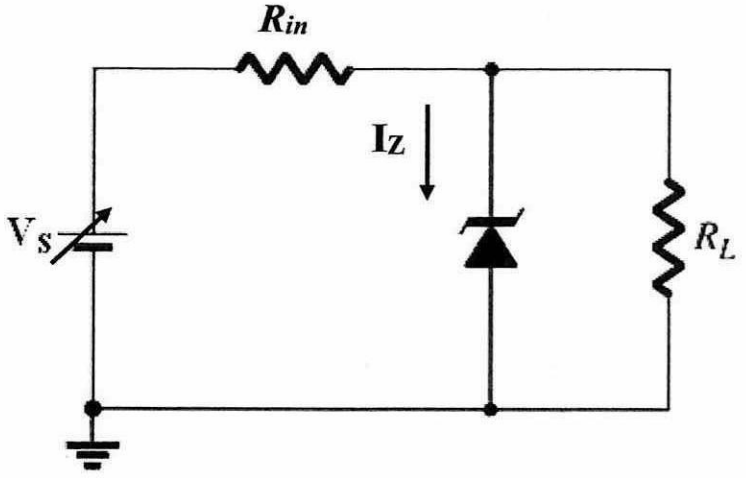
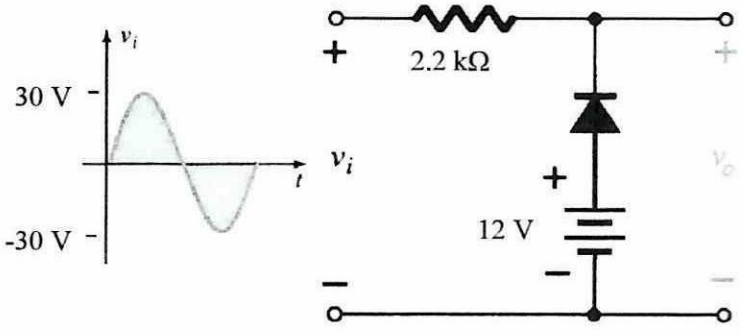
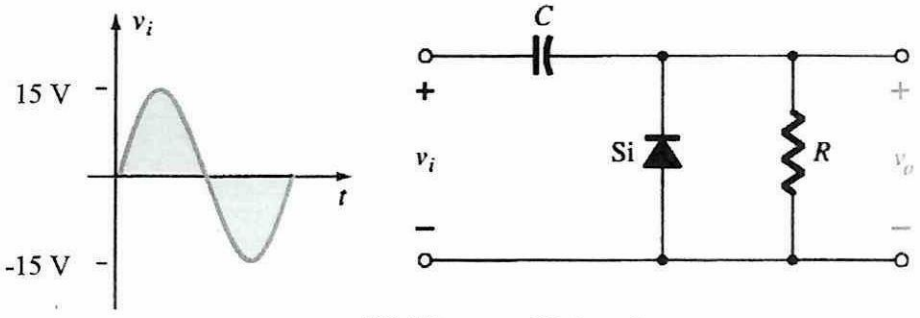


Figure Q2(a)



(i) Clipper Network



(ii) Clamper Network

Figure Q2(b)

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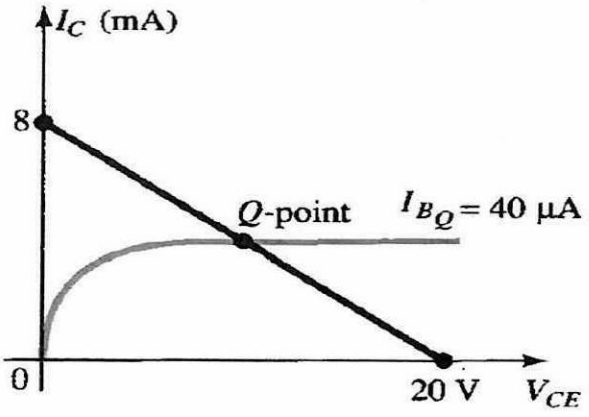
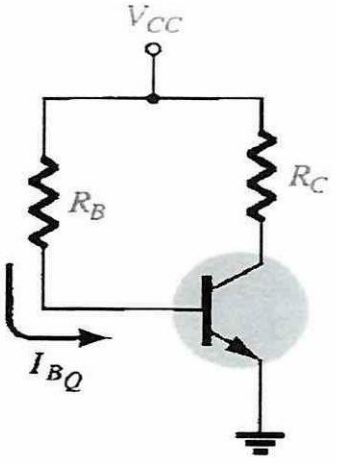


(i)



(ii)

Figure Q3(a)

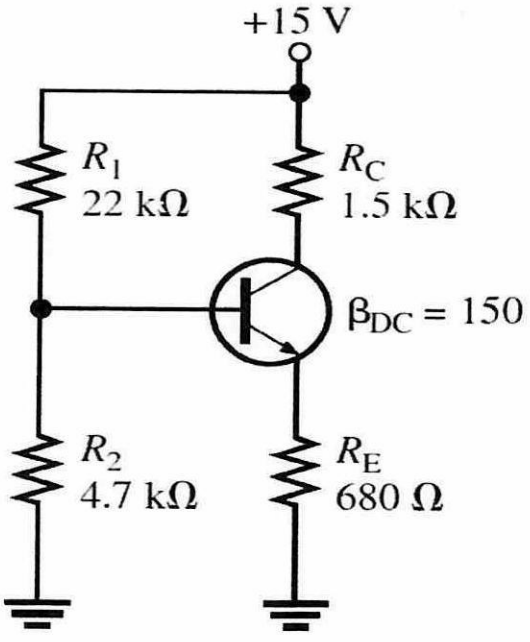


Figure Q3(b)

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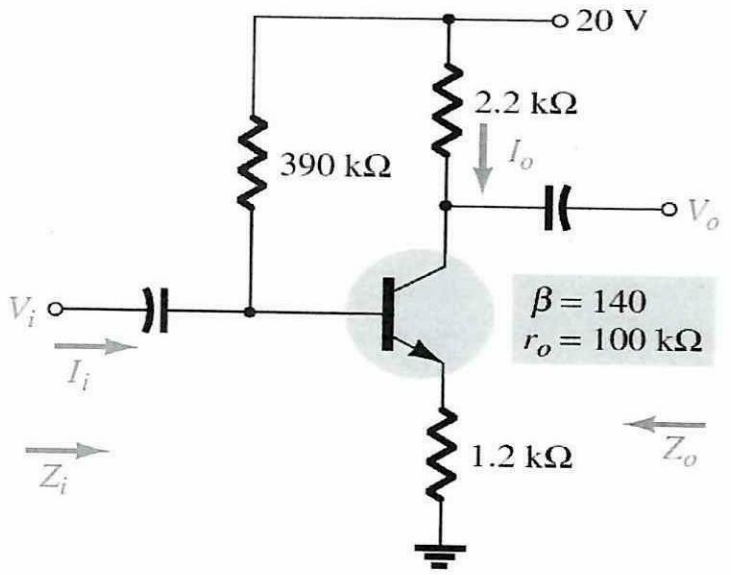

Figure Q3(c)

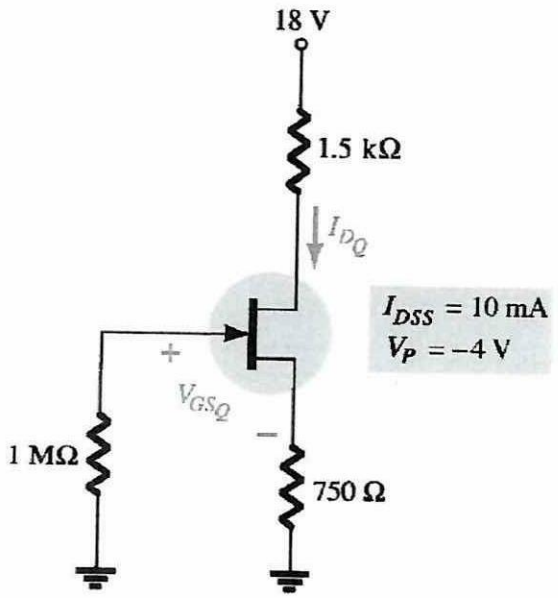

Figure Q4(b)

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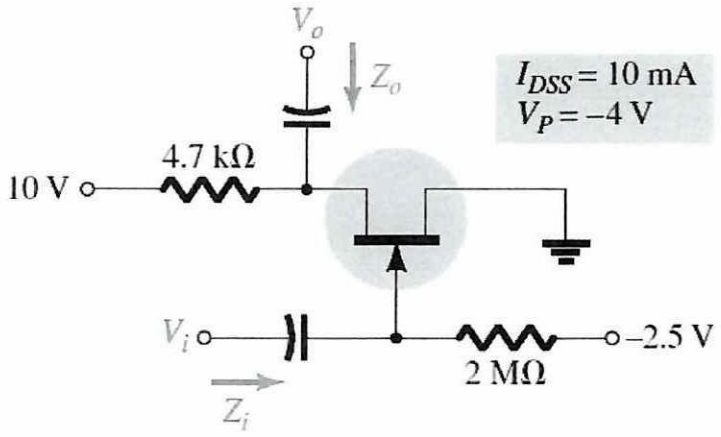

Figure Q4(c)

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