Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2022/2023

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BIC 10503
PROGRAMME CODE	:	BIS / BIP/ BIW/ BIM
EXAMINATION DATE	:	FEBRUARY 2023
DURATION	:	3 HOURS
INSTRUCTION	1.	ANSWER **ALL** QUESTIONS.
	2.	THIS FINAL EXAMINATION IS CONDUCTED VIA **CLOSED BOOK**.
	3.	STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK.

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) List **TWO (2)** benefits of Twos Complement in arithmetic operations.

(2 marks)

(b) (i) Convert $A10F_{16}$ into binary.

(2 marks)

(ii) Convert the result in **Q1(b)(i)** into Twos Complement.

(2 marks)

(c) Compute $1011_2 \times 1101_2$ using Unsigned Binary Multiplication approach. Show each step with the contents of registers: Multiplicand (M), Multiplier (Q), C and A, as well as its operation.

(5 marks)

(d) Derive the logic expression from the Truth Table in **Table Q1(d)**.

Table Q1(d)

B	C	D	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(5 marks)

(e) Derive the Boolean Function for each of the following Truth Tables using Karnaugh Map.

(i)

A	B	F
0	0	1
0	1	1
1	0	1
1	1	1

(2 marks)

(ii)

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(2 marks)

Q2 (a) The hexadecimal value, $30A79847_{16}$ is stored in location 1000 in a byte-addressable machine. Illustrate the memory contents for each of the following systems. Note that you may depict the memory as a column of boxes, where each box represents a single byte.

(i) Big-Endian.

(4 marks)

(ii) Little-Endian.

(4 marks)

(b) In a single-address processor, immediate and direct addressing methods are used. If the ALU output is 8 bits and memory size is 4 kB, what would be the maximum possible number of instructions in this processor?

(6 marks)

(c) Explain a major advantage for each of the following addressing modes.

(i) Immediate Addressing.

(2 marks)

(ii) Register Addressing.

(2 marks)

(iii) Stack Addressing.

(2 marks)

Q3 (a) Discuss **TWO (2)** important reasons why a processor requires a set of registers to execute programs.

(4 marks)

(b) Explain the purpose of the following register functions.

(i) User-visible registers.

(2 marks)

(ii) Control and status registers.

(2 marks)

(c) Assume a machine needs to run an instruction as below.

```
ADD R2, R1, 5
```

Illustrate and explain the fetch cycle based on the instruction.

(6 marks)

(d) Consider two instructions as below.

```
ADD R1, R2, R3
SUB A, R1
```

The CPU to run the instructions employ a 5-stage pipeline consisting of Fetch Instruction (FI), Decode Instruction (DI), Fetch Operands (FO), Execute Instruction (EI), and Write Operand (WO). Note that each stage requires one clock cycle. Answer the following questions.

(i) Illustrate the scenario with a timing diagram.

(2 marks)

(ii) Discuss your answer in **Q3(d)(i)**.

(4 marks)

Q4 (a) Explain the function of the following registers.

(i) Memory Address Register (MAR)

(1 mark)

(ii) Memory Buffer Register (MBR)

(1 mark)

(iii) Program Counter (PC)

(1 mark)

(iv) Instruction Register (IR)

(1 mark)

(b) Describe the micro-operations involved during the fetch cycle.

(4 marks)

(c) Compare and contrast between microprogrammed and hardwired implementation of a control unit.

(6 marks)

(d) In your opinion, which technique in **Q4(c)** is more appropriate for a high-performance computer that could perform complex calculations at high speeds? Justify your answer.

(6 marks)

- END OF QUESTIONS –