Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(ONLINE)
SEMESTER II
SESSION 2021/2022

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEJ30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2022
DURATION	:	3 HOURS

INSTRUCTION

1. ANSWER ALL QUESTIONS
2. THIS FINAL EXAMINATION IS AN **ONLINE** ASSESSMENT AND CONDUCTED VIA **CLOSED BOOK.**
3. STUDENTS ARE **PROHIBITED** TO CONSULT THEIR OWN MATERIAL OR ANY EXTERNAL RESOURCES DURING THE EXAMINATION CONDUCTED VIA CLOSED BOOK

THIS QUESTION PAPER CONSISTS OF **TWENTY FIVE (25)** PAGES

SECTION A (OBJECTIVE QUESTIONS)

OBJECTIVE PART 1: 20 QUESTIONS, 9 RANDOM QUESTIONS FOR EACH STUDENT

Q1 In which mode the operand is placed in one of 8-bit or 16-bit general purpose registers?
a) Immediate addressing
b) Register mode
c) Implied addressing
d) Register Indirect

(1 mark)

Q2 Zero address instruction is designed with implied addressing mode.
a) True
b) False
c) Can be true or false
d) Cannot say

(1 mark)

Q3 What is the postfix expression for the corresponding infix expression?
a + b * c + (d * e)

a) abc*+de*+
b) abc+*de*+
c) a+bc*de+*
d) abc*+(de)*+

(1 mark)

Q4 In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____
a) EA = 5+R1
b) EA = R1
c) EA = [R1]
d) EA = 5+[R1]

(1 mark)

Q5 What is the effective address for MUL 5(R1, R2)
a) 5+R1+R2
b) 5+(R1*R2)
c) 5+[R1]+[R2]
d) 5*([R1]+[R2])

(1 mark)

Q6 _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
a) Relative
b) Indirect
c) Index with Offset
d) Immediate

(1 mark)

Q7 Which register is used to store the value of arithmetic and logical operation?
a) arithmetic register
b) accumulator
c) logical register
d) controlled

(1 mark)

Q8 Built-in set of machine codes instructions of computer are called
a) instruction set
b) transfer of data
c) logical operations
d) logical set

(1 mark)

Q9 Specific purpose storage location is termed as
a) register
b) executed register
c) timed register
d) sequenced register

(1 mark)

Q10 Two main types of branch instructions are/is
a) conditional branch
b) unconditional branch
c) logical branch and conditional branch
d) conditional branch and unconditional branch

(1 mark)

Q11 Most of the time, computer instructions are divided into
a) function code
b) instruction code
c) operand and instruction code
d) function code and operand

(1 mark)

Q12 Counter that holds instruction fetched from store during decoding and execution is called
a) current instruction register
b) program instruction counter
c) sequence instruction register
d) programming register

(1 mark)

Q13 Ordered set of instructions that are carried out by a computer is called _____
a) programs
b) machine
c) machine code
d) programming languages

(1 mark)

Q14 Binary code which gives an actual instruction is called

a) instruction code
b) logical code
c) function code
d) address

(1 mark)

Q15 In instruction format, address of any data location is said to be
a) function code
b) instruction code
c) operand
d) logical code

(1 mark)

Q16 Sequence control register is also known as
a) program counter
b) instruction counter
c) sequence register
d) controlling register

(1 mark)

Q17 Counter that holds addresses of next fetched instruction is called
a) sequence control register
b) program counter
c) temporary register and program counter
d) sequence control register and program counter

(1 mark)

Q18 Instructions that are programmed to make decisions are termed as
a) branch instructions
b) programmed instruction
c) logical instruction
d) arithmetic instruction

(1 mark)

Q19 If a processor clock rated as 2500 million cycles per second, then its' clock period is
a) 4×10^{-10}
b) 4×10^{-9}
c) 4×10^{-6}
d) 4×10^{-3}

(1 mark)

Q20 What is the postfix expression for the following infix expression?
a / b ^ c – d

a) abc^/d-
b) ab/cd^-
c) ab/^cd-
d) abcd^/-

(1 mark)

OBJECTIVE PART 2: 20 QUESTIONS, 9 RANDOM QUESTIONS FOR EACH STUDENT

Q1 The main job of the interrupt system is to identify the _____ of the interrupt.
a) signal
b) device
c) source
d) peripherals

(1 mark)

Q2 The interrupts that are caused by software instructions are called _____
a) exception interrupts
b) normal interrupts
c) hardware interrupts
d) controlled interrupt

(1 mark)

Q3 In Daisy Chaining Priority, the device with the highest priority is placed at the _____.
a) first position
b) last position
c) can be placed anywhere
d) depend on device

(1 mark)

Q4 To overcome the lag in the operating speeds of the I/O device and the processor we use
a) buffer space
b) status flag
c) interrupt signal
d) exceptions

(1 mark)

Q5 Reads/writes requests to I/O devices, are called _____.
a) input request
b) output request
c) I/O request
d) peripheral request

(1 mark)

Q6 The interrupt-request line is a/an _____ along which the device is allowed to send the interrupt signal.
a) data line
b) control line
c) address line
d) none of them

(1 mark)

Q7 The method of accessing the I/O devices by repeatedly checking the status flags is called_____
a) program-controlled I/O

b) memory-mapped I/O
c) I/O mapped
d) none of the mentioned

(1 mark)

Q8 Interrupts initiated by an instruction is called as _____.
a) internal
b) external
c) hardware
d) software

(1 mark)

Q9 In memory mapped I/O _____
a) the I/O devices and the memory share the same address space
b) the I/O devices have a separate address space
c) the memory and I/O devices have an associated address space
d) a part of the memory is specifically set aside for the I/O operation

(1 mark)

Q10 A part of the memory which is specifically set aside for the I/O operation is called __
a) star bus structure
b) multiple bus structure
c) single bus structure
d) node to node bus structure

(1 mark)

Q11 The advantage of I/O mapped devices to memory mapped is _____
a) the former offers faster transfer of data
b) the devices connected using I/O mapping have a bigger buffer space operand and instruction code
c) the devices must deal with fewer address lines
d) no advantage as such

(1 mark)

Q12 Input and output devices are notified of a read or write operation by _____
a) pending an extra bit of the address
b) enabling the read or write bits of the devices
c) raising an appropriate interrupt signal
d) sending a special signal along the BUS

(1 mark)

Q13 The time between the receival of an interrupt and its' services is _____
a) interrupt delay
b) interrupt latency
c) cycle time
e) switching time

(1 mark)

Q14 The device which starts the data transfer is called _____
a) transactor
b) slave
c) distributor

d) initiator

(1 mark)

Q15 The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?

a) exception
b) signal handling
c) interrupts
d) DMA

(1 mark)

Q16 The process wherein the processor constantly checks the status flags is called as

a) polling
b) inspection
c) reviewing
d) echoing

(1 mark)

Q17 Which of the following groups consists of only input devices?

i) Mouse
ii) Keyboard
iii) Monitor
iv) Touchpad

a) i, ii, and iii
b) ii, iii, and iv
c) i, ii, and iv
d) i, ii, iii and iv

(1 mark)

Q18 From amongst the following given scenarios determine the right one to justify interrupt mode of data transfer

i) Bulk transfer of several kilobyte
ii) Moderately large data transfer of more than 1kb
iii) Short events like mouse action
iv) Keyboard inputs

a) i and ii
b) ii
c) i,ii and iv
d) iv

(1 mark)

Q19 How can the processor ignore other interrupts when it is servicing one?

i) By turning off the interrupt request line.

ii) By disabling the devices from sending the interrupts.
iii) By using edge-triggered request line

a) i and ii
b) ii and iii
c) i and iii
d) i ,ii and iii

(1 mark)

Q20 Which one of the following is true about a CPU having a single interrupt request line and single interrupt grant line?

i) Neither vectored nor multiple interrupting devices is possible.
ii) Vectored interrupts are not possible but multiple interrupting devices are possible.
iii) Vectored interrupts are possible and multiple interrupting devices are not possible.
iv) Both vectored and multiple interrupting devices are possible.

a) iii
b) iv
c) i and iv
d) iii and iv

(1 mark)

OBJECTIVE PART 3: 20 QUESTIONS, 9 RANDOM QUESTIONS FOR EACH STUDENT

Q1 Which of these does not happen in the Fetch stage?
a) the Program Counter is incremented by 1
b) the value in the Program Counter is sent to memory on the address bus
c) the value returned from memory on the data bus is stored in the current instruction register
d) the value returned from memory is added to the value in the accumulator.

(1 mark)

Q2 Which of these is NOT a bus in the CPU?
a) address bus
b) data bus
c) control bus
d) execute bus

(1 mark)

Q3 Which of these happens in the Execute stage?
a) The Program Counter is incremented by 1
b) The value in the Current Instruction Register is decoded
c) The value in the Accumulator is stored in memory
d) The data at the address in the Program Counter is fetched from memory

(1 mark)

Q4 What happens immediately after the Program Counter has been copied into the Memory Address Register (MAR)?
a) The data is returned from memory into the Memory Data Register (MDR)
b) The MAR is sent to memory along the address bus
c) The instruction in the Instruction Register (IR) is decoded
d) The data in the Accumulator is copied into the MDR

(1 mark)

Q5 What happens immediately after the Memory receives an address on the address bus in the Fetch stage?
a) Memory returns the data at the given address along the data bus
b) Memory updates the data at the given address using the value supplied on the data bus
c) A second address is sent to memory
d) The Program Counter is incremented

(1 mark)

Q6 What happens immediately after data is returned to the Memory Data Register (MDR) from Memory in the Fetch stage?
a) Data from the MDR is copied into the Current Instruction Register
b) Data from the MDR is copied into the Program Counter
c) Data from the MDR is copied into the Accumulator
d) Data from the MDR is sent back to memory along the data bus

(1 mark)

Q7 What happens in the Decode stage after data is copied into the Instruction Register (IR)?

a) The control unit decodes the IR to determine the data value
b) The ALU executes the instruction in the IR
c) The data in the IR is copied into the Memory Address Register
d) The data in the IR is added to the value in the Accumulator

(1 mark)

Q8 Which of these is NOT something that can happen in the Execute stage?

a) Data from Memory is copied into the Accumulator
b) Data from the Accumulator is copied into the Memory
c) Data from Memory is added to the Accumulator, and the result is stored in the Accumulator
d) The Program Counter is copied into the Memory Address Register

(1 mark)

Q9 Which of these busses is unidirectional?

i) Address bus
ii) Control bus
iii) Data bus
iv) Counter bus

a) i and ii
b) i and iii
c) ii and iii
d) iii and iv

(1 mark)

Q10 The first stage of the Fetch-Decode-Execute cycle is:

a) the instruction is fetched from the RAM
b) the instruction is decoded so that it can be executed
c) any processing is done using the ALU
d) the Program Counter is incremented

(1 mark)

Q11 The second stage of the Fetch-Decode-Execute cycle is:

a) the instruction is fetched from the RAM
b) the instruction is decoded so that it can be executed
c) any processing is done using the ALU
d) the Program Counter is incremented

(1 mark)

Q12 The third stage of the Fetch-Decode-Execute cycle is:

a) the instruction is fetched from the RAM
b) the instruction is decoded so that it can be executed
c) any processing is done using the ALU
d) the Program Counter is incremented

(1 mark)

Q13 What is the program counter job?

a) to count the programs
b) it stores instruction
c) it contains the memory address of the next instruction to be loaded
d) it carries out the calculation

(1 mark)

Q14 The CPU process instructions by using _____
a) Fetch Decode Execute cycle
b) parallel processing
c) machine code
d) control bus

(1 mark)

Q15 Sequence control register is also known as
a) program counter
b) instruction counter
c) sequence register
d) controlling register

(1 mark)

Q16 Which of these does **not** affect CPU performance?
a) Clock Speed
b) Number of Cores
c) Cache Size
d) Number of instructions in a program

(1 mark)

Q17 The results of calculations is stored in _____
a) Memory Address Register
b) Instruction Register
c) Program Counter
d) General Purpose Register

(1 mark)

Q18 Which register holds instructions/data temporarily after it is brought to the processor from main memory?
a) Memory Address Register
b) Instruction Register
c) Program Counter
d) General Purpose Register

(1 mark)

Q19 Where would the operation "AND" be performed?
a) Arithmetic Logic Unit
b) Accumulator
c) Cache
d) Control Unit

(1 mark)

Q20 Which of these happen during the execution part of the fetch-decode-execute cycle?
a) Fetching the address

b) Program Counter is incremented
c) Arithmetic Operations performed
d) Main Memory is addressed

(1 mark)

OBJECTIVE PART 4: 20 QUESTIONS, 9RANDOM QUESTIONS FOR EACH STUDENT

Q1 How many bytes does a memory can be contained if it has 1500 words of 256 bits each?
a) 48 Kbyte
b) 48000 Kbyte
c) 384 Kbyte
d) 384000 Kbyte

(1 mark)

Q2 How many 64kB RAM chips are needed to provide a memory capacity of 512kB?
a) 8
b) 64
c) 128
d) 256

(1 mark)

Q3 The effectiveness of the cache memory is based on the property of _____
a) Memory size
b) Locality of reference
c) Memory localization
d) None of the mentioned

(1 mark)

Q4 The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____
a) Memory sticks
b) Blue-ray devices
c) CMOS
d) Flash memory

(1 mark)

Q5 Cache memory acts between_____
a) CPU and RAM
b) RAM and ROM
c) CPU and Hard Disk
d) Primary Storage and Secondary Storage

(1 mark)

Q6 Which of the following is not a form of memory?
a) Cache
b) Instruction Opcode
c) Instruction Register
d) General Purpose Register

(1 mark)

Q7 A dynamic RAM consists of
a) 6 transistors
b) 2 transistors and 2 capacitors
c) 1 transistor and 1 capacitor
d) none of these

(1 mark)

Q8 Four memory chips of 16 x 4 size have their address bases connected. The system will be of size

a) 64 x 64
b) 16 x 16
c) 32 x 16
d) 256 x 2

(1 mark)

Q9 The stack pointer in the microprocessor is a _____
a) 16 bits register those points to stack memory locations
b) 32-bit accumulator
c) memory location in the stack
d) flag register used for the stack

(1 mark)

Q10 What is the purpose of cache?
a) Performs Arithmetic and Logical operations
b) Decodes and directs instructions to be carried out
c) Stores frequently used data and instructions
d) Processes graphical functions

(1 mark)

Q11 Data and instructions in use are stored in the _____
a) processor
b) hard disk drive
c) embedded system
d) main memory

(1 mark)

Q12 What acts as an intermediary between the processor and main memory?
a) peripheral device
b) user
c) cache
d) clock

(1 mark)

Q13 What is held in cache?
a) All programming instructions
b) Commonly used instructions and data
c) Instructions that haven't been processed
d) Data that hasn't been used recently

(1 mark)

Q14 In terms of computer memory, what is meant by the term "volatile"?
a) It retains its content when power is cut
b) It loses its contents when power is cut
c) It is not stable and should not be used
d) Memory chips can overheat

(1 mark)

Q15 Which statement best describes RAM?
a) Fast, permanent storage
b) Slow, volatile storage

c) Fast, volatile storage
d) Slow, permanent storage

(1 mark)

Q16 Which statement best describes ROM?
a) A flash memory chip that contains a small amount of non-volatile memory
b) A memory store containing a large amount of volatile memory
c) A register within the CPU responsible for storing memory addresses
d) A memory store containing a small amount of volatile memory

(1 mark)

Q17 In comparison with static RAM memory, the dynamic RAM memory has _____
a) lower bit density and higher power consumption
b) higher bit density and lower power consumption
c) lower bit density and lower power consumption
d) none of these

(1 mark)

Q18 When is Virtual Memory needed or used by a computer?
a) When RAM becomes full because of too many programs running at once
b) When ROM is too small and struggles to store the Operating System
c) When users wish to store data on an external server such as 'the cloud'
d) When chosen by the user or computer administrator

(1 mark)

Q19 Disadvantage of dynamic RAM over static RAM is
a) higher power consumption
b) variable speed
c) need to refresh the capacitor charge every once in two milliseconds
d) lower packing density

(1 mark)

Q20 Where is ROM usually found inside a computer?
a) Inside the CPU
b) As part of the hard drive
c) On the motherboard
d) With the DVD drive

(1 mark)

OBJECTIVE PART 5: 19 QUESTIONS, 9 RANDOM QUESTIONS FOR EACH STUDENT

Q1 What is meant by a multi-core processor?

a) A single CPU with multiple core components
b) A multi-CPU system
c) A CPU that has been overclocked
d) A CPU that has a faster clock speed

(1 mark)

Q2 If the number of cores goes from dual-core to quad-core, what effect does this have on performance?
a) Performance decreases
b) The maximum number of instructions executed per second quadruples
c) The maximum number of instructions executed per second halves
d) The maximum number of instructions executed per second doubles

(1 mark)

Q3 If the processing speed goes from 1GHz to 4GHz, what effect does this have on performance?
a) The maximum number of instructions executed per second doubles
b) The maximum number of instructions executed per second halves
c) The maximum number of instructions executed per second quadruples
d) The maximum number of instructions executed per second quarters

(1 mark)

Q4 Which of the following is/are advantage of pipelining?
a) Instruction throughput increases.
b) Faster ALU can be designed when pipelining is used.
c) Pipelining increases the overall performance of the CPU.
d) All of the above.

(1 mark)

Q5 Hazard in pipeline are as follows except_____
a) data hazard
b) instruction hazard
c) structural hazard
d) execution hazard

(1 mark)

Q6 When multiple instructions are overlapped during execution of program, then function performed is called _____.
a) pipelining
b) multitasking
c) hardwired control
d) multiprogramming

(1 mark)

Q7 The situation where in the data of operands are not available is called _____
a) stock
b) deadlock
c) data hazard

d) structural hazard

(1 mark)

Q8 Which of the following best describes pipelining?
a) Processing multiple instructions at once
b) Routing a network connection around a firewall
c) Receiving data from multiple servers at the same time
d) Accessing multiple memory modules from a single CPU

(1 mark)

Q9 Each stage in pipelining should be completed within ____ cycle.
a) 1
b) 2
c) 3
d) 4

(1 mark)

Q10 If a unit completes its task before the allotted period, then
a) it'll perform some other tasks in the remaining time
b) it'll remain idle for the remaining time
c) its time gets reallocated to different task
d) none of the mentioned

(1 mark)

Q11 The periods of time when the unit is idle is called as _____.
a) stall
b) delay
c) null
d) branch

(1 mark)

Q12 To increase the speed of memory access in pipelining, we make use of _____.
a) cache
b) buffers
c) special purpose registers
d) special memory locations

(1 mark)

Q13 The contention for the usage of a hardware device is called as _____.
a) stalk
b) deadlock
c) structural hazard
d) none of the mentioned

(1 mark)

Q14 The fetch and execution cycles are interleaved with the help of _____.
a) clock
b) special unit
c) control unit
d) modification in processor architecture

(1 mark)

Q15 To increase the speed of memory access in pipelining, we make use of _____
a) special memory locations
b) special purpose registers
c) cache
d) buffers

(1 mark)

Q16 Pipelining is a unique feature of _____
a) CISC
b) RISC
c) ISA
d) ANNA

(1 mark)

Q17 Which of the following is disadvantage of pipelining?
a) Cycle time of the processor is reduced.
b) The design of pipelined processor is complex and costly to manufacture.
c) The instruction latency is less
d) Increase the CPU performance

(1 mark)

Q18 The average number of steps taken to execute the set of instructions can be made to be less than one by implementing_____ operation.
a) ISA
b) superscalar
c) non-pipeline
d) RISC

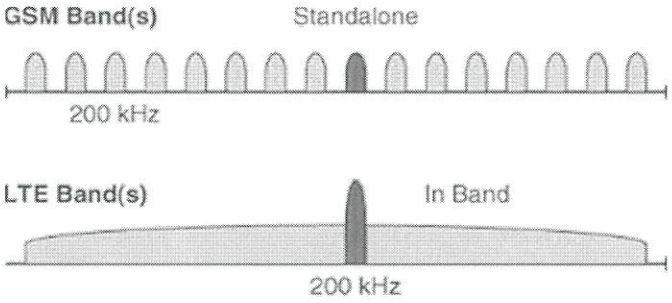
(1 mark)

Q19 If some combination of instructions cannot be accommodated because of resource conflicts, the processor is said to have a _____
a) data hazard
b) structural hazard
c) pipeline hazard
d) stall

(1 mark)

OBJECTIVE PART 6: 10 QUESTIONS, 5 RANDOM QUESTIONS FOR EACH STUDENT

Q1



Above figure shows an example of _____
a) LoRaWAN Architecture
b) NB-IoT Deployment Options
c) Neural Network
d) ZigBee IP Protocol

(1 mark)

Q2 Internet of Things will digitize the world by connecting:
i) Data
ii) People
iii) Process
iv) Search

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv

(1 mark)

Q3 Characteristics of a Smart Object including:
i) Actuator
ii) Power Source
iii) Sensors
iv) Tiny Low-Cost Computer

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q4 _____ are devices that detect and respond to changes in an environment. They're embedded in smart phones and an integral part of the Internet of Things.
a) Barcode
b) RFID
c) Sensors
d) ZigBee

(1 mark)

Q5 With the use of Internet of Things,

i) a manufacturer cannot repair more than 3 faults at one go.
ii) a manufacturer can order the required parts to be used to make the repairs.
iii) a manufacturer can set up an appointment to repair the fault.
iv) a manufacturer can integrate the data coming from various devices.

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q6 IoT is the network of physical objects embedded with _____, which enables these objects to collect and exchange data.

i) electronics
ii) network connectivity
iii) sensors
iv) software

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q7 What technologies have made IoT possible?

i) Artificial Intelligence
ii) Connectivity
iii) Low-cost sensors
iv) Machine learning

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q8 Which of the following fields is not part of the top application in Internet of Things?

i) Daily Life
ii) Health and Security
iii) Traffic Monitoring
iv) Transport and Logistics

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) None of the stated

(1 mark)

Q9 The IoT reference model published by the IoT World Forum including the following levels:

i) Application
ii) Connectivity
iii) Data Accumulation
iv) Edge Computing

a) i, ii, and iii
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q10 What is most likely sensor that used by online transportation business (e.g., Food Panda, Grab, Uber)?

a) Barcode Scanner
b) GPS Module
c) Passive Infrared Sensor
d) RFID Tag

(1 mark)

SECTION B (SUBJECTIVE QUESTIONS)

Q51 (a) Briefly explain the steps needed in executing a program.

(5 marks)

(b) Assume that a memory is executing this instruction:

M[834] <- M[832] * M[833]

and the Opcode representation is as in **Table Q51(b)**.

Table Q51(b): Opcode representation

Opcode	Instruction
0_H	HALT
1_H	LOAD
2_H	STORE
3_H	MUL

The initial Memory, Program Counter (PC), Accumulator (AC) and Instruction Register (IR) value is as in **Figure Q51(i)**.

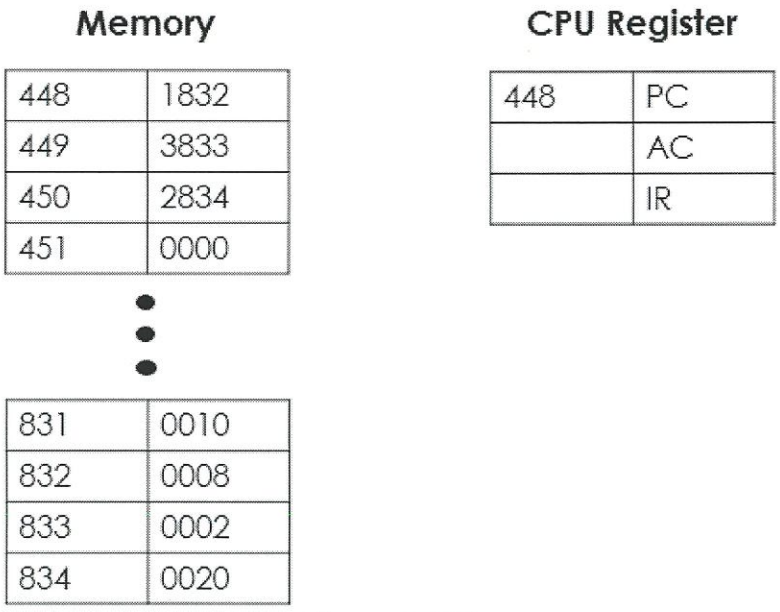


Figure Q51(i)

After fetch, decode, execute, and write back process for that instruction, identify the final value for a, b, c, d, e, f, and g (refer to **Figure Q51(ii)**).

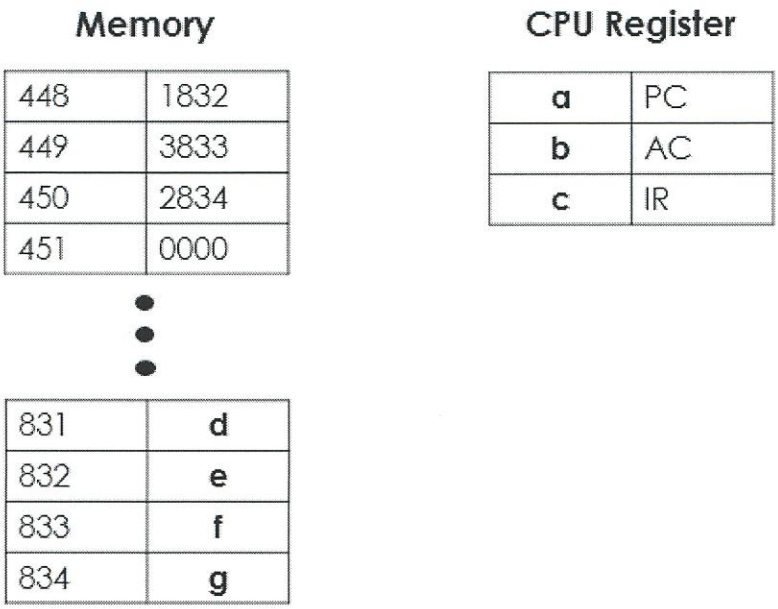


Figure Q51(ii)

(5 marks)

(c) Assume that location Y in ADD Y instruction is 105 and it carries a value of 13_d. By ignoring the black box determine the appropriate value in the white blank box of **Table Q51(c)**.

Table Q51(c)

Steps	RTN	PC	IR	MAR	MDR	AC
initial		101		101	ADD y	2
FETCH	MAR ← PC	101		101	ADD y	2
	IR ← MDR	101		101	ADD y	2
	PC ← PC + 1			101	ADD y	2
DECODE	decode IR					
EXECUTE	AC ← MDR + AC					

(5 marks)

Q52 (a) Determine two differences between Primary storage and Secondary storage.

(2 marks)

(b) Consider a system with multiple level memory as in **Table Q52(b)**.

Table Q52(b)

Component	Value
Cache Hit Rate	90 %
Cache Hit Time	5 ns
Off Chip Cache Hit Rate	96 %
Off Chip Cache Hit Time	10 ns
Main Memory Hit Rate	99.8 %
Main Memory Hit Time	60 ns
Main Memory Miss Penalty	10 000 ns

(i) Calculate the Average Memory Access Time for this system.

(6 marks)

(ii) Calculate the Global Miss Rate for this system.

(2 marks)

(iii) Assume that the size of the Off Chip Cache is increased in a way that the Global Miss Rate is reduced up to 20%. Calculate the new value for Global Miss Rate and Global Hit Rate.

(2 marks)

(c) Assume that a Direct Mapping Function is apply on a memory system with 24-bit address. The cache has 16384 blocks, each storing 4 words. Calculate its tag, block, and word size.

(3 marks)

Q53 One way to improve the performance of a CPU is by arranging the hardware such that more than one operation can be performed at the same time. Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction takes place in a pipelined processor. Given CPU M has a set of instructions to run as shown in **Listing Q53**. The instruction format for instructions in **Listing Q53** is shown in **Figure Q53**. The execution of each instruction involves five steps (Fetch Instruction, Decode, Read Operand, Execute and Write Result). For each step, the execution time is 1 cycle.

```
MOV  #1, R01
MOV  #5, R03
MOV  #3, R01
ADD  R01, R03
```

Listing Q53

Operation	Source operand	Destination Operand

Figure Q53

(a) Predict the value in register R03 at the end of **Listing Q53** instructions.

(2 marks)

(b) Illustrate the execution of instructions in **Listing Q53** if the CPU M implements no-pipelined method.

(3 marks)

(c) Illustrate the execution of instructions in **Listing Q53** if the CPU M implements pipeline method.

(3 marks)

(d) Compare the total execution time for non-pipelined with pipeline method. Calculate the speedup factor.

(2 marks)

(e) Instructions in **Listing Q53** has been simulated in CPU simulator, however the result in register R03 given by the simulator is 6, different with the prediction value. By using your answer in **Q53(c)**, explain this situation by relating with hazard that may happen in pipeline method.

(3 marks)

(f) Suggest modification that should be done to the **Listing Q53** so that the result in register R03 is the same as predicted.

(2 marks)

Q54 Smart city Malaysia aims at addressing urban issues and challenges towards achieving the three main pillars of competitive economy, sustainable environment, and enhanced quality of life. The smart city trend is supported by the technological breakthrough of the Fourth Industrial Revolution (Industry 4.0), including the use of Internet of Things (IoT), Cloud Computing, Open Data and Big Data Analytics. As an engineer, you are asked to give ideas regarding the implementation of smart city traffic in Cyberjaya. Draw the smart city traffic architecture to present your ideas.

(5 marks)

- END OF QUESTIONS –