Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER I
## SESSION 2021/2022

| | | |
|---|---|---|
| COURSE NAME | : | COMPUTER ARCHITECTURE |
| COURSE CODE | : | BIC 10503 |
| PROGRAMME CODE | : | BIS / BIP/ BIW/ BIM |
| EXAMINATION DATE | : | JANUARY / FEBRUARY 2022 |
| DURATION | : | 3 HOURS |
| INSTRUCTION | : | 1. ANSWER **ALL** QUESTIONS |
| | | 2. THIS FINAL EXAMINATION IS CONDUCTED ONLINE AND CLOSE BOOK . |

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

**Q1** (a) Illustrate **THREE (3)** Input Output Techniques for input of a block of data.
(5 marks)

(b) Discuss the techniques in **Q1(a)**.
(12 marks)

(c) State **THREE (3)** functions about External Devices.
(3 marks)

**Q2** (a) Represent the following floating-point number in a 32-bit format.

0.000000000000001985

(5 marks)

(b) Elaborate the requirements to compute $10010_2$ x $11001_2$ using Booth's algorithm based on the following aspects.

(i) Arithmetic operations.
(3 marks)

(ii) Registers.
(4 marks)

(c) Construct a truth table for the following logic circuit in **Figure Q2** by considering the input in **Table Q2.**

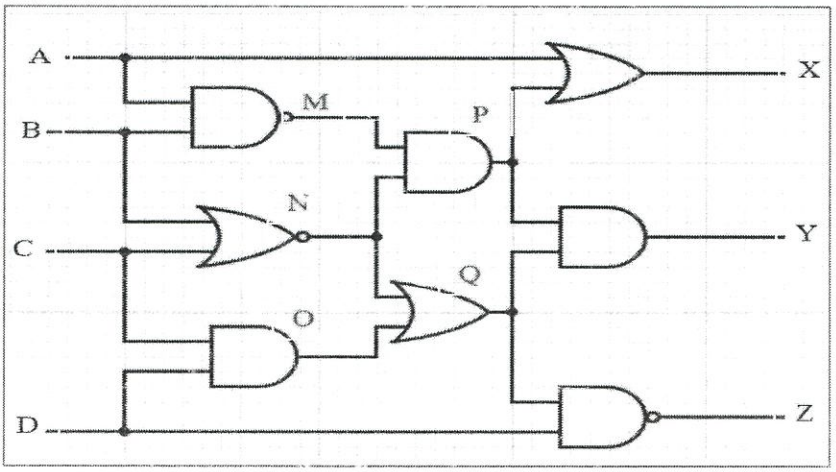


**Figure Q2**

**Table Q2**

| A | B | C | D |
|---|---|---|---|
| 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |

(8 marks)

**Q3** **Table Q3** shows a list of opcodes, each with its description.

**Table Q3**

| Opcode | Description |
|---|---|
| ADD | Compute sum of two operands |
| SUB | Compute difference of two operands |
| MUL | Compute product of two operands |
| DIV | Compute quotient of two operands |
| MOVE | Transfer word or block from source to destination |
| STORE | Transfer word from processor to memory |
| LOAD | Transfer word from memory to processor |

Write a machine-language program in symbolic form to compute : $X = ((L+M) \times N) - (O/P)$ for each the following machines.

(i) 3- Address machines

(5 marks)

(ii) 2- Address machines

(7 marks)

(iii) 1- Address machines

(8 marks)

**Q4** (a) How does pipelining improve the performance of a processor?

(2 marks)

(b) **Figure Q4** shows a sequence of Intel x86 assembly language.

```
ADD EAX, ECX ;load register EAX with the contents of ECX
             ;plus the contents of EAX
MOV EBX, EAX ;load EBX with the contents of EAX
```

**Figure Q4**

(i) Elaborate **FOUR (4)** steps of an instruction cycle to run the codes.

(8 marks)

(ii) Illustrate a four-stage pipeline using a timing diagram for the instructions. Assume that each stage requires 1 clock cycle.

(10 marks)

**Q5** (a) Based on situations below, explain the control signal sequence:

(i) Transfer the address of PC to Memory Address Register (MAR).

(2 marks)

(ii) Transfer the words in memory to Memory Buffer Register (MBR).

(4 marks)

(b) Write micro operation for the following instructions:

(i) `ADD AC, X`

(ii) `ADD X,(A)`

(iii) `MOV CX, (CHAR)`

(12 marks)

(c) State **FOUR (4)** common registers used in micro operation fetch cycle.
(2 marks)

**- END OF QUESTIONS -**