UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(ONLINE)
SEMESTER II
SESSION 2020/2021

COURSE NAME	:	IC PACKAGING
COURSE CODE	:	BEJ 43503
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2021
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS **OPEN BOOK EXAMINATION**

THIS QUESTION PAPER CONSISTS OF **THREE (3)** PAGES

Q1 (a) (i) Briefly explain the microsystem and microelectronics packaging.
(7 marks)

(ii) Imagine you are one of the package design engineer and you have a functional Integrated Circuits (ICs) that will be ready soon to be packaged. Design the package complete suitable for military operation with **FIVE (5)** importance criteria or requirement that should be taken or fulfill before package the ICs.
(10 marks)

(b) Gordon Moore predicts that the transistors on a chip double every 24 months. This increased product functionality because of more transistors on the single ICs. Analyze **FOUR (4)** complexity and challenges in perspective of packaging to support Moore's law.
(10 marks)

Q2 (a) Die Attach (also known as Die Mount or Die Bond) is the process of attaching the silicon chip to the die pad or die cavity of the support structure (e.g., the leadframe) of the semiconductor package.

(i) With aid of diagram, sketch structure of Die Attach and explain the process of Epoxy attach method.
(5 marks)

(ii) List **THREE (3)** common failure mechanisms related to Die Attach (DA) process.
(3 marks)

(b) (i) Explain and sketch the structure of IC dual-in-line package and label the parts of die, wire bonding, bond pad and lead frame.
(10 marks)

(ii) Analyse the differences between the methods of Thermo-compression and Thermo-sonic wire bonding.
(7 marks)

Q3 (a) Briefly explain the semiconductor packaging process as below.

(i) Deflash, Trim, Form and Singulate (DTFS)
(4 marks)

(ii) Sealing
(3 marks)

(iii) Electrical Testing
(3 marks)

(b) Design and explain the package technology for Pin-Through-Hole (PTH), Flip Chip and Surface-Mount-Technology.

(15 marks)

Q4 (a) Packaging is needed in all ICs, which are classified into Through-Hole Technology (THT) and Surface Mount Technology (SMT). Both packages has its own unique packaging process flow.

(i) Explain **THREE (3)** primary requirements that should be taken into consideration before IC assembly process.

(6 marks)

(ii) Analyze **FOUR (4)** advantages of Surface Mounting Technology (SMT) and the difference between THT and SMT.

(12 marks)

(b) (i) Explain general process of molding transfer.

(4 marks)

(ii) Give **THREE (3)** common failure mechanisms that occur during wafer marking and sealing process.

(3 marks)

- END OF QUESTIONS -