Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(TAKE HOME)
SEMESTER II
2020/2021

COURSE NAME	:	SMART SENSOR AND EMBEDDED SYSTEM
COURSE CODE	:	MET 10603
PROGRAMME CODE	:	MET
EXAMINATION DATE	:	JULY 2021
DURATION	:	4 HOURS
INSTRUCTION	:	ANSWER **ALL** THE QUESTIONS **OPEN BOOK EXAMINATION**

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 **(a)** Compare the differences between sc_thread and sc_method module implementations in SystemC.

(4 marks)

(b) Convert the following Verilog-based system of a revised 32-bit T flip flop into its SystemC equivalent. Write your solution using the code templates provided.

(12 marks)

```
module tff (clock, reset, t, q)
input clk, rst, t, en;
output reg [0:31] q;

always @(posedge clock or reset)
begin
        if (reset)
                q <=1'b0;
        else
        if (t)
                q <= ~q;
else
                q<= q;
end
endmodule
```

Template:

tff.h

```
#include <systemc.h>
SC_MODULE(tff){
```

tff.cpp

```
#include "tff.h"
void tff :: tff_method(){
```

(c) Compare a co-processor and an accelerator.

(2 marks)

(d) A central processing unit in System on Chip (SoC) A and a hardware accelerator able to execute instruction P faster. The accelerator able to run program M, which has 60pct instruction P on SoC A, 2 times faster than without an accelerator. Determine the factor of improvement for instruction P in SoC A.

(7 marks)

Q2 **(a)** Explain at least one financial reason why SoC are so prevalent in today's world from a financial standpoint.

(6 marks)

(b) SoC design involves dividing work between hardware and software as well as for deciding the number of general-purpose and custom processors and co-processors to be used. Outline the main factors that influence these design decisions and the associated manual partition of envisaged workload over these resources.

(6 marks)

(c) Distinguish between uniform memory access (UMA) and non-uniform memory access (NUMA) systems.

(2 marks)

(d) Describe the differences between physical, virtual, and logical memory.

(6 marks)

(e) Justify the reason for Network-On-Chip (NoC) gradually replacing the bus-based interconnection.

(5 marks)

Q3 **(a)** The clock period decreases with the increases of pipeline stages. Justify **TWO (2)** reason why processors do not have thousands or millions of pipeline stages.

(4 marks)

(b) Consider an instruction pipeline with four stages (each with a combinational circuit only). The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in **Figure Q3(b).** Analyze the approximate speed up of the pipeline in steady-state under ideal conditions when compared to the corresponding non-pipelined implementation.

(7 marks)

(c) Modify the pipeline stages in **Figure Q3(b)** to increase the throughput of the pipeline at least by 40%.

(7 marks)

(d) In an instruction pipeline with five stages without any branch prediction: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Operand Write (OW). The stage delays for IF, ID, OF, EX and OW are 5 ns, 7 ns, 10 ns, 8 ns and 4 ns, respectively. An intermediate storage buffer is used between the stages and has a delay of 1 ns. A program consisting of 12 instructions I1, I2, …, I12 is executed in the pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program,

(i) Deduce the phase-time diagram and time needed to complete the program
(5 marks)

(ii) Identify the type of hazard that can be eliminated in this pipeline design.
(2 marks)

Q4 **(a)** Theoretically, as more and more cores are placed on chip, it can make sense to connect them with some sort of interconnection network to support core-to-core communication. Assume that you have a 6-core chip that you want to program. Propose the most suitable number of cores to solve a given problem with the following details:

- You can use as few as 1 core or as many as 6 cores
- The problem requires 450,000 iterations of a main loop to complete
- Each loop iteration requires 100 clock cycles
- Any startup overhead can be ignored
- If more than 1 core is used to solve a problem, communication overhead specified in **Table Q4(a)** must be added to the total execution time.

(10 marks)

(b) Consider a system-on-chip (SoC) consisting of a video accelerator to support multimedia applications. This system can do video decoding via a video accelerator. Suggest the location of input, intermediate, and output frames to and the accelerator being stored.

(4 marks)

(c) A sensor is a device, module, machine, or subsystem whose purpose is to detect events or changes in its environment and send the information to other electronics, frequently a computer processor.

(i) Classify **THREE (3)** types of sensors with their area of detection, specification and applications.

(3 marks)

(ii) Sketch the block diagram of a smart sensor system for a smart farming application and suggest the type of sensor suitable for the system.

(3 marks)

(iii) Based on part Q4(c)((ii), design your circuit for smart farming. In the design, use Arduino Uno shown in **Figure Q4(c)**. Show all the pin connections for each of the sensors and output used in the design.

(5 marks)

- END OF QUESTIONS -

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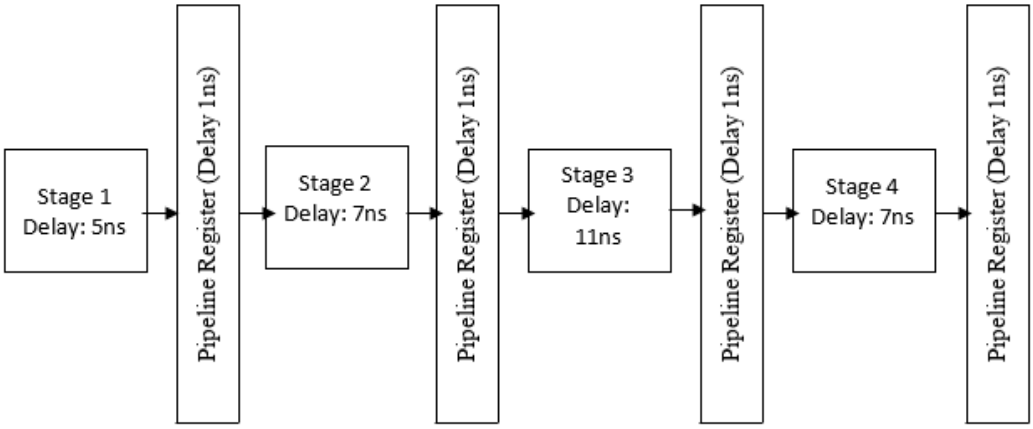

Figure Q3(b): Delays for the stages and for the pipeline registers

Table Q4(a): Communication overhead

Number of cores used to solve problem	Communication overhead per iteration
1	0 cycles
2	10 cycles
3	20 cycles
4	30 cycles
5	40 cycles
6	50 cycles

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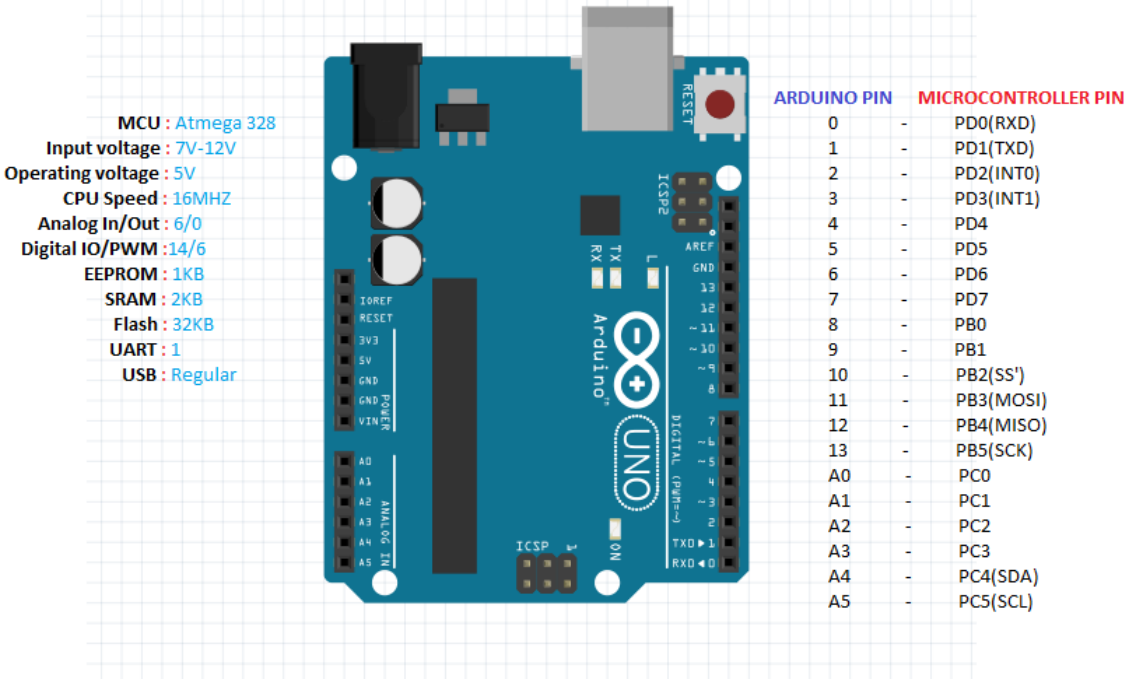

Figure Q4(c): Arduino Uno