

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION ONLINE **SEMESTER I SESSION 2020/2021**

COURSE NAME

ELECTRICAL AND ELECTRONICS

TECHNOLOGY

COURSE CODE

: BDX 10203

PROGRAMME CODE :

BDX

EXAMINATION DATE : JANUARY 2021/FEBRUARI 2021

DURATION

: 3 HOURS

INSTRUCTION

ANSWERS THREE (3) QUESTIONS FROM

PART A AND TWO(2) QUESTIONS FROM

PART B

THIS QUESTION PAPER CONSISTS OF EIGHT (8) PAGES

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PART A

Q1	(a)	Define and give explanation on the factor that contributes these parameters and law:		
		(i) (ii)	Conductance	(2 marks) (2 marks)
		(iii)	Olun's Law	(2 marks)
	(b)	Aluminum wire with 7.5m long is connected in parallel with copper wire of 6m leas shown in Figure Q1(a) . When a current of 5 A is passed through the parallel circ it is found that the current in the aluminum wire is 3A. The diameter of the alumin wire is 1mm. Determine the diameter of the copper wire. (7 mag)		
	(c)	Find the Q1(b)		ın Figure (7 marks)
Q2	(a)	Explai	n the steps required to perform nodal analysis in electric circuits	(5 marks)
	(b)	_	nodal analysis, determine the current flows in I1 and the power consu	
				10 marks)
×	(c)		ate the direction and magnitude of the current through the 5 Ω resistor A and B of Figure 2 (b) by using nodal voltage method.	r between



(10 marks)

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Q3 Thévenin is a useful tool to simplify and analyze a complex electronic circuit.

(a) Explain in detail the steps to do Thévenin analysis.

(4 marks)

(b) Figure Q3(a) shows a complex electronics circuit. Use Thévenin method to find the Thévenin equivalent circuit with respect to 1nF capacitor. Hint: use superposition to find Vth.

(6marks)

(c) Find the Norton Equivalent Circuit with respect to the $3k\Omega$ resistor in the middle of the circuit as shown in **Figure Q3(b)**. The $3k\Omega$ resistor itself should not be part of the equivalent circuit that you compute.

(6 marks)

(d) Based on the result that you compute in Q3(c) determine the Thévenin equivalent circuit of this circuit.

(4 marks)

Q4 (a) Determine the resonance for the network shown in Figure Q4(a)

(4 marks)

- (b) A parallel plate capacitor is charged to 100V. Its plate separation is 2mm and the area of each of its plate is 120cm². Calculate and account for the increase or decrease of stored energy when plate separation is reduced to 1mm
 - (i) at constant voltage

(3 marks)

(ii) at constant charge

(3 marks)

- (c) Three capacitors $2\mu F$, $3\mu F$ and $5\mu F$ are connected in series and charged from a 900Vdc supply.
 - (i) Find the voltage across each capacitors.

(5 marks)

(ii) They are then disconnected from the supply and reconnected with all the +ve plate connected together and all the -ve plates connected together. Find the voltages across the combinations and the charge on each capacitor after reconnections. Assume perfect insulation.

(5 marks)



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PART B

- Q5 (a) The maximum value of the alternating voltage and current are 400V and 20A respectively in a circuit connected to a 50Hz supply and these quantities are sinusoidal. The instantaneous values of the voltage and current are 283V and 10A respectively at t=0 both increasing positively.
 - (i) Write down the expression for voltage and current at time, t.

(4 marks)

(ii) Sketch the sine waveform that reflect to the expression produced in (i).

(4 marks)

(iii) Determine the power consumed in the circuit.

(4 marks)

- (b) The half cycle of an alternating signal is as shown in **Figure Q5(a)**. It increase uniformly from zero at 0° to F_m at α °, remains constant from α ° to $(180-\alpha)$ °. The signal is then decreases uniformly from F_m at $(180 \ \alpha)$ ° to zero at 180°.
 - (i) Calculate the average values of the signal.

(3 marks)

(ii) Evaluate the effective values of the signal.

(5 marks)

Q6 (a) One UTHM graduate has found a new property in material X where it exhibits the capability to detect the presence of a magnetic field. Describe five features required by Material X in order to make it as the right candidate for magnetic sensing.

(8 marks)

(b) Apply DeMorgan's Theorems to the following Boolean expression and simplify it.

$$Y - (A + \overline{\overline{BC}} + CD) + \overline{\overline{BC}}$$

(4 marks)

(c) Reduce the function specified in the truth table of **Table Q6(a)** to its minimum sum-of-product (SOP) form using a Karnaugh map. Hence, develop the logic circuit using NAND gates only.

(8 marks)

-END OF QUESTIONS

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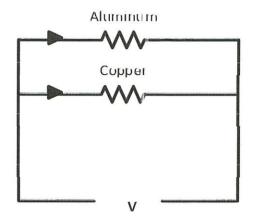


Figure Q1(a)

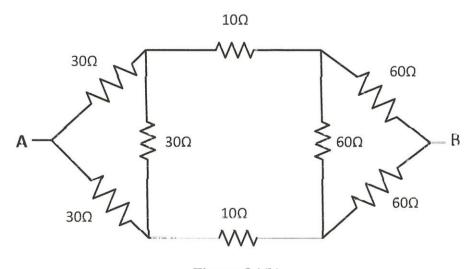


Figure Q1(b)



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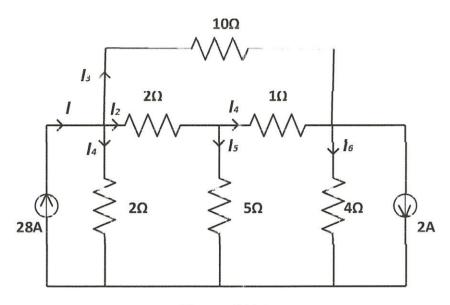


Figure Q2(a)

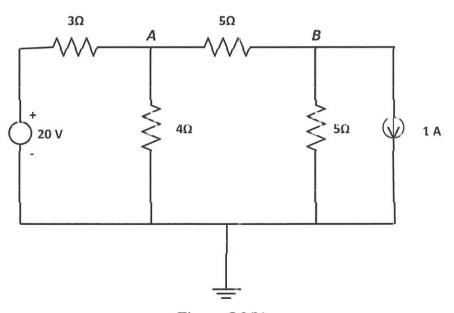


Figure Q2(b)

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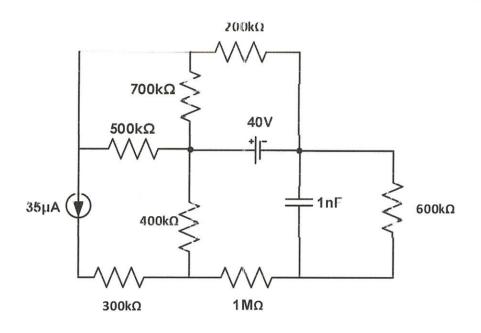


Figure Q3(a)

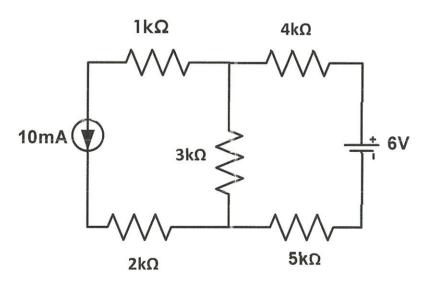


Figure Q3(b)



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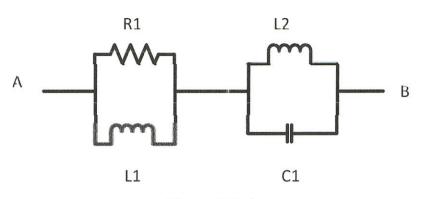


Figure Q4(a)

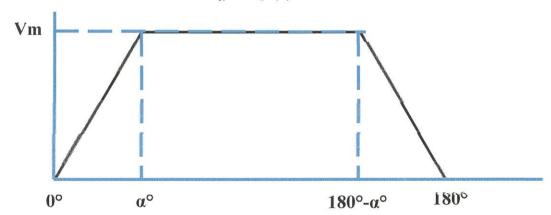


Figure Q5(a)

INPUTS	OUTPUT
ABC	X
0 0 0	1
0 0 1	1
010	()
011	1
1 0 0	1
1 0 1	1
1 1 0	0
111	1

TABLE Q6(a)

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