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UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
(ONLINE)
SEMESTER II
SESSION 2019/2020**

COURSE NAME : COMPUTER ARCHITECTURE
COURSE CODE : BIT 20303
PROGRAMME CODE : BIT
EXAMINATION DATE : JULY 2020
DURATION : 2 HOURS 30 MINUTES
INSTRUCTION : 1. ANSWER ALL QUESTIONS.
2. PLEASE MAKE SURE TO
CLICK "SAVE ANSWER"
BUTTON FOR SUBJECTIVE
QUESTIONS. OBJECTIVE
QUESTIONS ARE SAVED
AUTOMATICALLY

THIS QUESTION PAPER CONSISTS OF FIVE (5) PAGES

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TERBUKA

Q1 (a) Show the 2's complement signed magnitude 8 bits representation of the following:

(i) $+54_{10}$ (3 marks)

(ii) -43_{10} (4 marks)

(b) Compute the following binary pairs and show your calculation.

(i) $1100\ 0100 + 0011\ 0110$ (2 marks)

(ii) 1110×1010 (3 marks)

(iii) $0111\ 1111 \div 11$ (4 marks)

(c) Complete the truth table in Table **Q1(c)** for the following logic circuit in the Figure **Q1(c)**.

(4 marks)

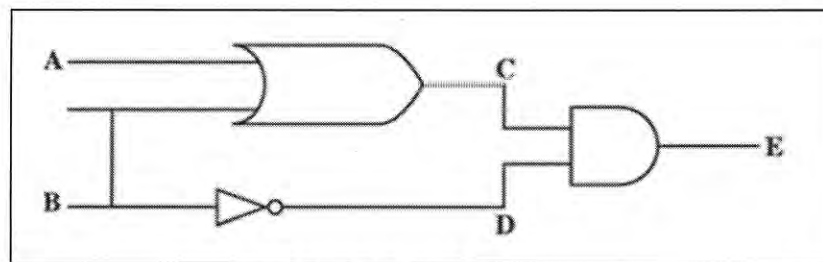


FIGURE Q1(c)

TABLE Q1(c)

| A | B | C | D | E |
|---|---|---|---|---|
| 0 | 0 | | | |
| 0 | 1 | | | |
| 1 | 0 | | | |
| 1 | 1 | | | |

Q2 Figure Q2 shows a list of opcodes, each with its description.

| | |
|------|-----------|
| ADD | Add |
| SUB | Subtract |
| MPY | Multiply |
| DIV | Divide |
| MOVE | Move data |

Figure Q2

Write a machine-language program in symbolic form to compute: $Y = (A - B) / (C + (D \times E))$ for the following machines.

- (a) 3-address machines (4 marks)
- (b) 2-address machines (5 marks)
- (c) 1-address machines (6 marks)
- (d) Based on answers in Q2(a), Q2(b), and Q2(c), analyze the impact of having fewer addresses per instruction. (5 marks)

- Q3**
- (a) Explain **FIVE (5)** processor tasks to form a complete instruction cycle. (10 marks)
 - (b) A processor is designed with a Memory Address Register (MAR), a Memory Buffer Register (MBR), a Program Counter (PC) and an Instruction Register (IR). It is required to run a machine instruction as below.

ADD R1, R0, 1

Based on the above statement, illustrate and explain the fetch cycle. (3 marks)

(c) **Figure Q3(c)** shows the execution of nine instructions in pipeline.

| | | Time → | | | | | | | | | | | | | |
|---------------|--|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| Instruction 1 | | FI | DI | CO | FO | EI | WO | | | | | | | | |
| Instruction 2 | | | FI | DI | CO | FO | EI | WO | | | | | | | |
| Instruction 3 | | | | FI | DI | CO | FO | EI | WO | | | | | | |
| Instruction 4 | | | | | FI | DI | CO | FO | EI | WO | | | | | |
| Instruction 5 | | | | | | EI | DI | CO | FO | EI | WO | | | | |
| Instruction 6 | | | | | | | FI | DI | CO | FO | EI | WO | | | |
| Instruction 7 | | | | | | | | FI | DI | CO | FO | EI | WO | | |
| Instruction 8 | | | | | | | | | FI | DI | CO | FO | EI | WO | |
| Instruction 9 | | | | | | | | | | FI | DI | CO | FO | EI | WO |

Figure Q3(c)

Illustrate a two-stage pipeline consisting fetch operation and execute operation to run four instructions.

(5 marks)

Q4 (a) Suggest **ONE (1)** suitable method in designing control unit for a computer that uses Graphics Processing Unit (GPU).

(2 marks)

(b) Give **FOUR (4)** reasons of your suggestion in **Q4(a)**.

(8 marks)



- (c) **Figure Q4(c)** shows a block diagram of the Control Unit. Explain its **FOUR (4)** inputs and its **TWO (2)** outputs.

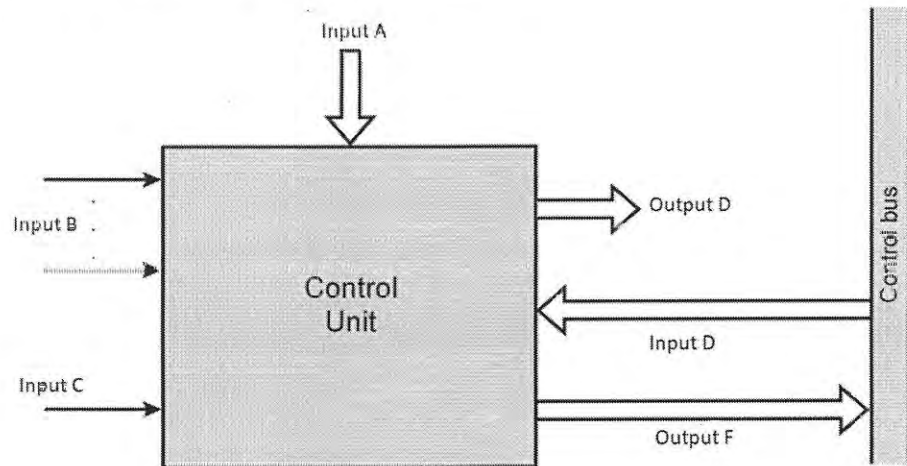


Figure Q4(c)

(10 marks)

- END OF QUESTIONS -

