UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(TAKE HOME)
SEMESTER II
SESSION 2019/2020

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JULY 2020
DURATION	:	6 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS. **OPEN BOOK EXAMINATION**

THIS QUESTION PAPER CONSISTS OF FIVE **(5)** PAGES

Q1 (a) Identify and explain the various ways to reduce the delay time of a CMOS inverter. Prove your explanation with the related formulae.

(3 marks)

(b) ICoN Sdn. Bhd. manufactured a total of 18,000 fully-functional dies in January 2019. The chip production uses 500 wafers that could accommodate 50 dies per wafer. Compute the average number of fully functional dies per wafer and average die yield.

(5 marks)

(c) Explain the following basic design rules in VLSI layout design and for each rule, draw an appropriate diagram to illustrate what is meant by the rule.

(i) size rule (2 marks)

(ii) separation rule (2 marks)

(iii) overlap rule (2 marks)

(d) **Figure Q1(d)** shows a stick diagram of logical circuit using fully complementary static CMOS.

(i) Analyse the figure and draw the electrically equivalent transistor level schematic of the stick diagram. Determine the logic equation for the output *OUT*.

(6 marks)

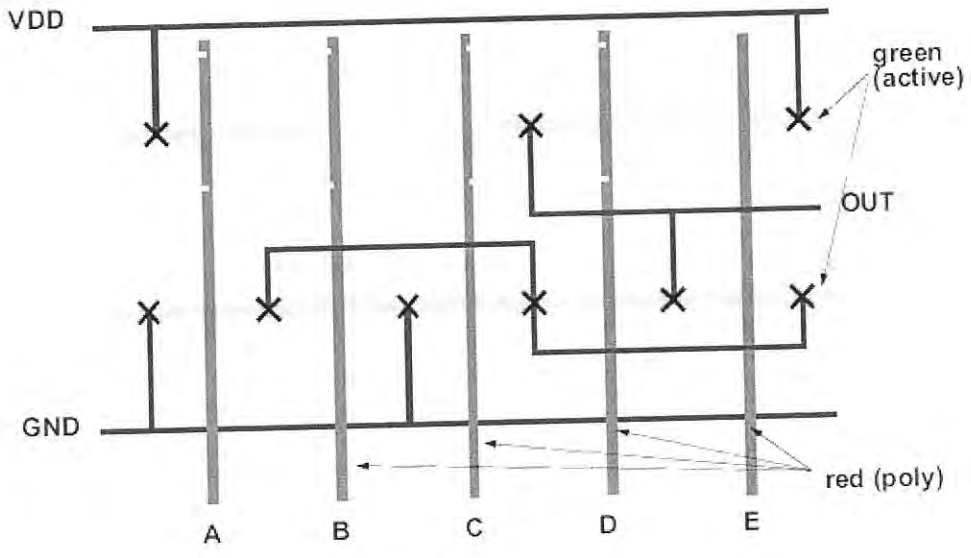

Figure Q1(d)

(ii) Transform the transistor logic circuit in answer **Q1(d)(i)** as a dynamic logic that can prevent a contention problem.

(5 marks)

Q2 (a) Design a fully complementary static CMOS circuit using minimum number of transistors to realize the following equation. The circuit need to have a minimum parasitic delay.

$$Y = \overline{A + (B + C) + D.E}$$

(10 marks)

(b) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability of an inverter. Assume that the minimum length for the transistor is 2λ and the mobility ratio of electron and holes is 2.

(10 marks)

(c) Calculate the minimum parasitic delay for the circuit.

(5 marks)

Q3 (a) List out the testing techniques for combinational circuit and explain stuck-at fault method.

(5 marks)

(b) Sensitize each path in the circuit in Figure **Q3(b)** to obtain a complete test set that comprises a minimum number of tests.

(20 marks)

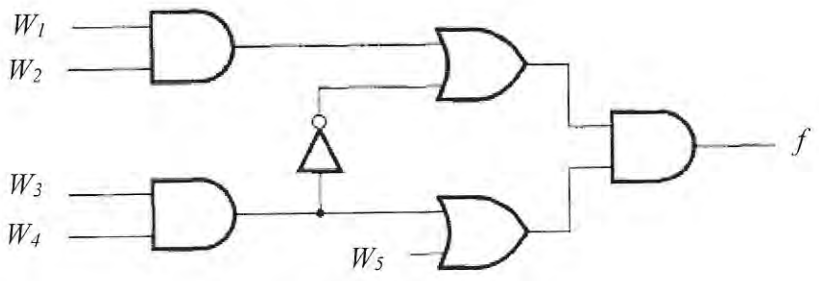

Figure Q3 (b)

Q4 (a) In sequential circuit, perfect timing is very crucial in determining the correct operation of the circuit. Explain the following timing parameters and illustrate the timing diagram that depict those parameters.

(i) Setup Time

(2 marks)

(ii) Output Delay Time

(2 marks)

(b) A two non-overlapping clock can be generated by using NOR-based structure like unclocked SR latch circuit.

(i) Illustrate the circuit of the two non-overlapping clock at gate level.

(4 marks)

(ii) Draw the circuit at transistor level using a full complementary static CMOS with a minimum number of transistors.

(5 marks)

(c) Figure **Q4(c)** show a SR clocked NOR based flip-flop gate circuit.

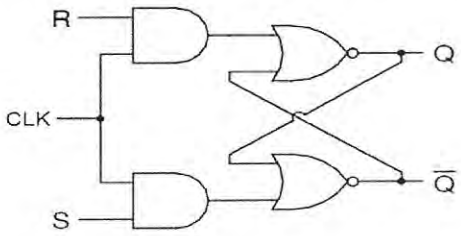

Figure Q4(c)

(i) Complete the timing diagram given in the **Figure Q4(c)(i)**. Assume that Q is at low level initially.

(4 marks)

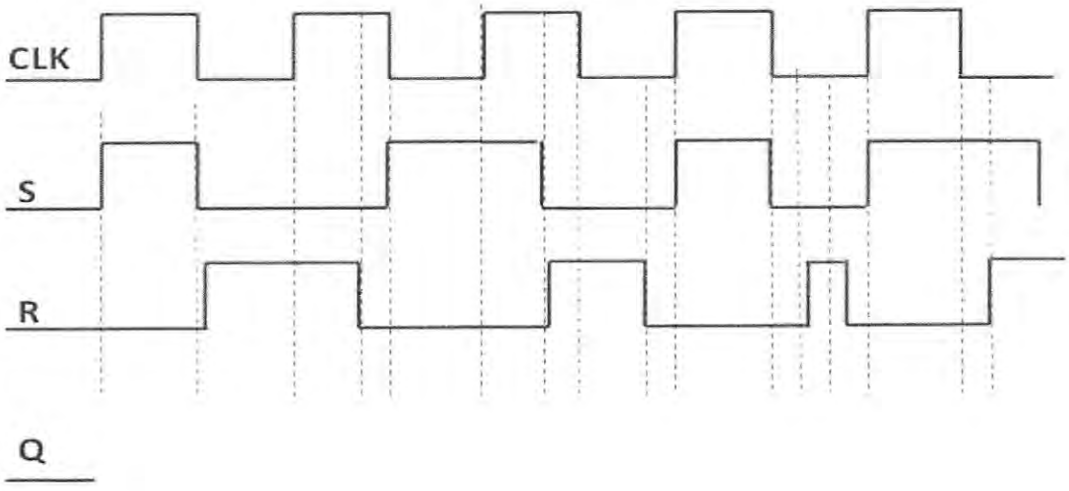

Figure Q4(c)(i)

(d) Draw transistor circuit for the logic circuit in **Figure Q4(c)** using minimum static CMOS.

(8 marks)

- END OF QUESTIONS -