UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(TAKE HOME)
SEMESTER II
SESSION 2019/2020

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEJ 10603/BEL 20303/BEV 10603
PROGRAMMECODE	:	BEJ / BEV
EXAMINATION DATE	:	JULY 2020
DURATION	:	5 HOURS
INSTRUCTION	:	ANSWERS **ALL** QUESTIONS. **OPEN BOOK EXAMINATION**

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) A jet aircraft employs a system for monitoring the rpm, pressure and temperature values of its engines using sensors that operates as follows:

Temperature sensor, T = 0 only when temperature < 200 F
Pressure sensor, P = 0 only when pressure < 220 psi
RPM sensor, R = 0 only when speed < 4800 rpm

Sensors output T, P and R will be 1 if they exceed their maximum limits or else 0. Pilot will be given a warning when the temperature of the engine is more than 200F and either engine pressure is more than 220 psi or the engine speed is less than 4800 rpm. Assume that a HIGH at output W activates the warning light.

(i) Obtain the truth table for this circuit.

(4 marks)

(ii) By using Karnaugh map, write the simplest Boolean expression for W.

(4 marks)

(iii) Draw the schematic diagram for W based on its Boolean expression in part **Q1(a)(ii)**.

(2 marks)

(b) Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number which are X_1 and X_0, representing that count in binary.

(i) Construct the truth table for this circuit.

(8 marks)

(ii) Find the minimize logic equations for output X_1 and X_0. Use the Karnaugh map and Boolean algebra to simplify the expressions.

(7 marks)

Q2 (a) **Figure Q2(a)** *shows how an eight-input multiplexer can be used to generate a four-*variable logic function, even though the multiplexer has only three SELECT inputs.

(i) Analyze and build the truth table for this circuit. (Hint: D is the MSB)

(12 marks)

(ii) Write the Boolean expression of this circuit. You do not need to simplify the expression.

(4 marks)

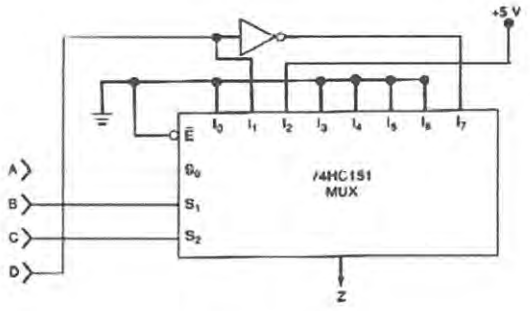


Figure Q2(a)

(b) Evaluate the output for a 4-bit compactor (74LS85) in **Figure Q2(b)** using given inputs of A0, A1, A2, A3, B0, B1, B2 and B3 below. The outputs are active-HIGH. (9 marks)

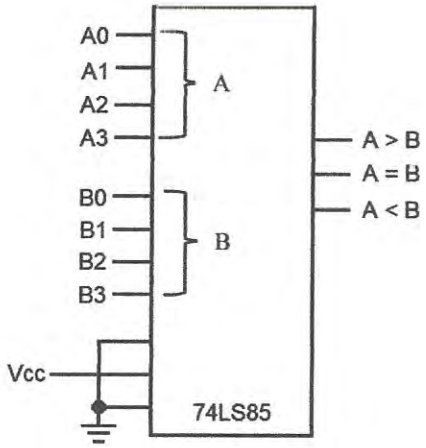
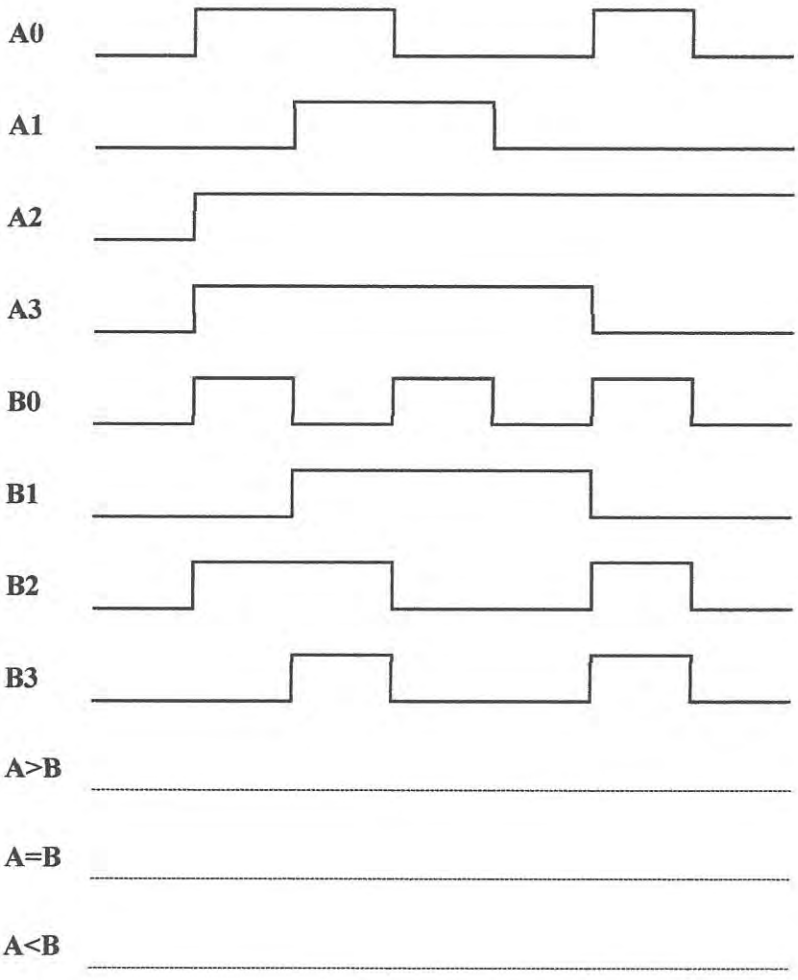


Figure Q2(b)



Q3 (a) **Figure Q3(a)** shows a BCD counter that produces a four-bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example after four pulses have occurred, the counter outputs are DCBA=0100_2=4_{10}. The counter resets to 0000 on the tenth pulse and starts counting over again. In other words, the DCBA outputs will never represent a number greater than 1001_2–9_{10}. Design the logic circuit that produces HIGH output whenever the count is 2, 3, or 9. Use K mapping and take advantage of the don't-care conditions.

(10 marks)

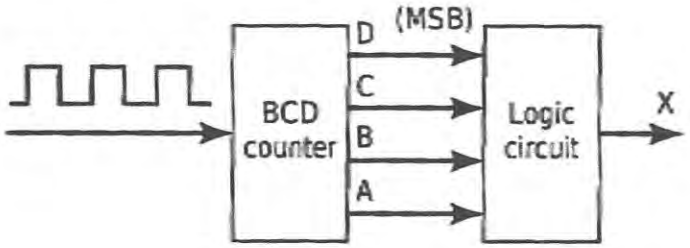


Figure Q3(a)

(b) **Figure Q3(b)(i)** shows a logic circuit that comprises of a JK, SC and D flip-flop. **Figure Q3(b)(ii)** shows the waveforms for signal CLK, X, Y, $\overline{CLR}$ and $\overline{PRE}$. Complete the timing diagram for Q_A, Q_B and Q_C in **Figure Q3(b)(ii)**. Assume that Q_A, Q_B and Q_C are at high level initially.

(10 marks)

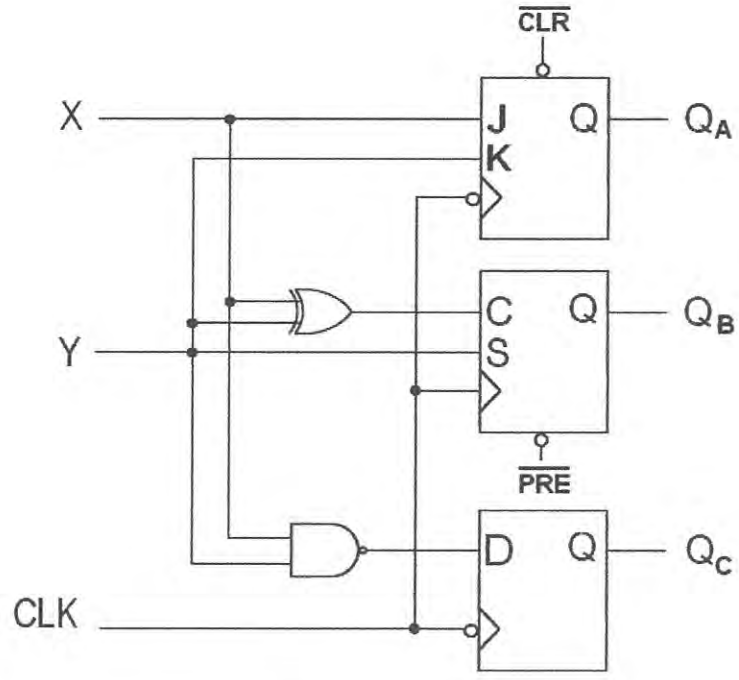


Figure Q3(b)(i)

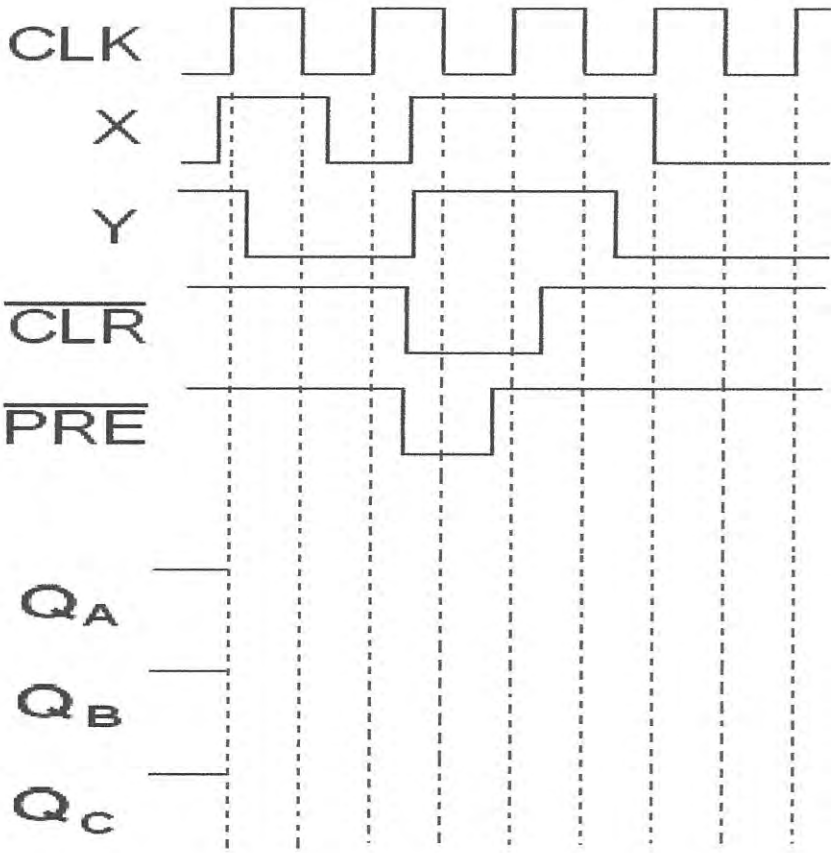


Figure Q3(b)(ii)

(c) Derive the implemented logic function from a multiplexer in **Figure Q3(c)**.

(5 marks)

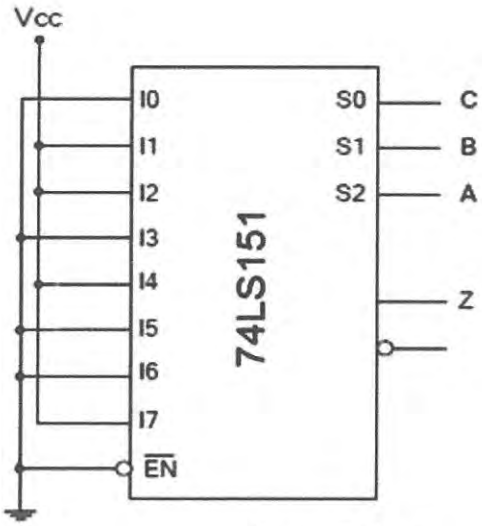


Figure Q3(c).

Q4 (a) The clock divider circuit has found immense application in multiple clock domain (MCD) systems like SoC (System on Chip) and GALS (Globally Asynchronous, Locally Synchronous).As an engineer, you are required to design a clock divider that can generate two frequencies, 12 kHz and 3 kHz from input frequency of 48 kHz. The clock divider circuit must be design using JK flip-flop.

(8 marks)

(b) **Figure Q4(b)** shows the waveforms for signal CLK and D, which are the inputs to D latch and a D positive going transition (PGT) flip-flop. CLK input goes into the EN input of the D latch. Complete the timing diagram for Q_{DL} as the output of D latch and Q_{DFF} as the output for D flip-flop Assume that $Q_{DL}$and Q_{DFF} are at low level initially.

(10 marks)

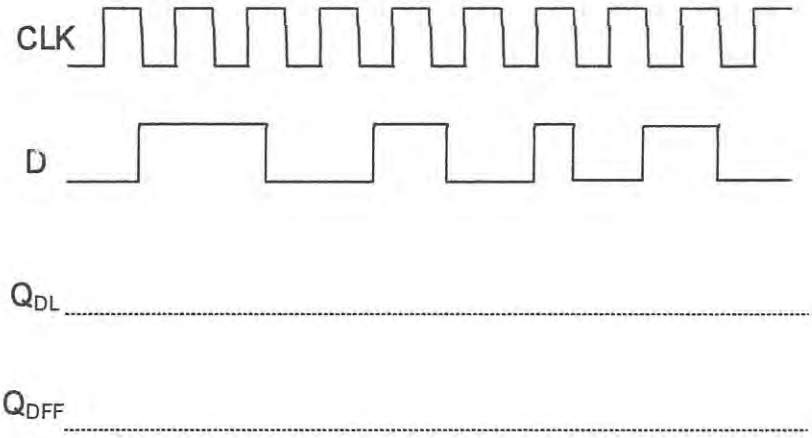


Figure Q4(b)

(c) **FigureQ4(c)(i)** shows a block diagram of a JK flip-flop. **Figure Q4(c)(ii)** illustrate the waveforms for signal CLK, J, K, $\overline{PRE}$ and $\overline{CLR}$. Complete the timing diagram for Q of JK Flip-flops. Identify and labelled the SET, RESET and HOLD states. Assume that Q at high level initially.

(7 marks)

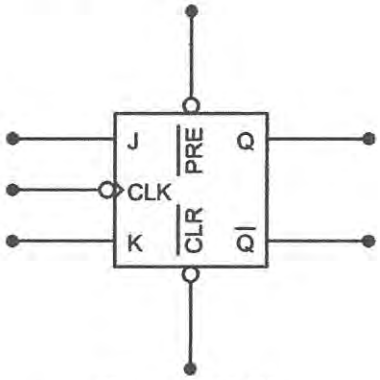


Figure Q4(c)(i)

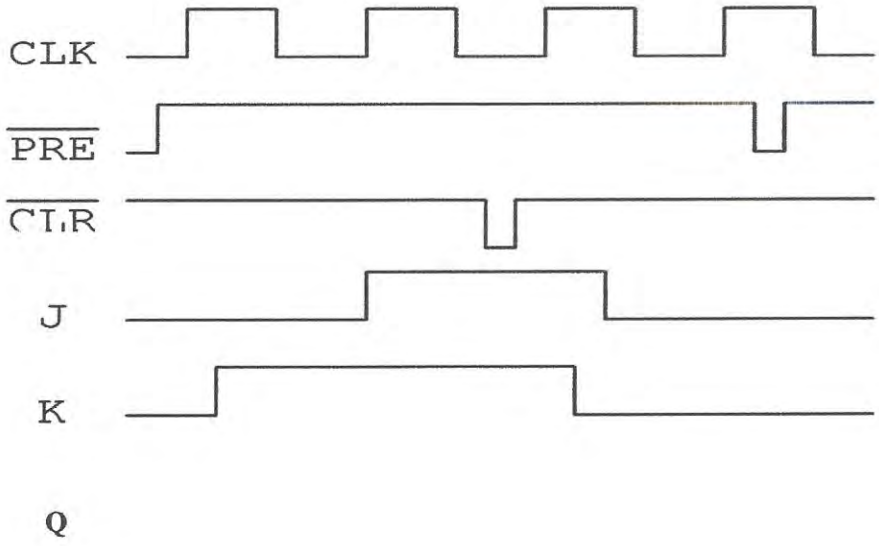


Figure Q4(c)(ii)

-END OF QUESTIONS -