UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
(TAKE HOME)
SEMESTER II
SESSION 2019/2020

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303/BEJ30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JULY 2020
DURATION	:	5 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS **OPEN BOOK EXAMINATION**

THIS QUESTION PAPER CONSISTS OF **TWELVE (12)** PAGES

SECTION A: 40 Objectives Questions (40 marks)

Q1 THREE (3) factors affect the performance of a computers are:
a) Hardware design, Instruction set, Compiler
b) Hardware design, Speed, Cost
c) Speed, Cost, Memory management
d) Speed, Cost, Compiler

(1mark)

Q2 Integrated circuit is on _____ generation in computer evolutions
a) First
b) Second
c) Third
d) Fourth

(1 mark)

Q3 The main board that consist of all components in a computer is called as:
a) hard drive
b) primary storage
c) motherboard
d) processor

(1 mark)

Q4 The ALU makes use of _____ to store the intermediate results.
a) accumulators
b) calculators
c) registers
d) stack

(1 mark)

Q5 The control unit controls other units by generating _____.
a) control signals
b) timing signals
c) traffic signals
d) transfer signals

(1 mark)

Q6 The main advantage of multiple bus organization over single bus is _____.
a) reduction in the number of cycles for execution.
b) increase in size of the registers
c) better connectivity
d) none of these

(1mark)

Q7 Data transfer between the main memory and the CPU register takes place through two registers namely _____.
a) MAR and MDR
b) MAR and Accumulator
c) accumulator and program counter
d) general purpose register and MDR

(1 mark)

Q8 The instruction, Add R1, R2 does _____.
a) Adds the value of R1 to R0 and stores in the temp register
b) Adds the value of R2 to the address of R1
c) Adds the values of both R1 and R2 and stores it in R1
d) Adds the value of R1 with a value in accumulator and stores it in R2

(1 mark)

Q9 Which register in the processor is single directional?
a) Hard Disk
b) MAR
c) Cache
d) RAM

(1 mark)

Q10 The operation of the processor's hardware components is governed by control signals. This control signal have TWO (2) basic approaches, there are:
a) Hardwired and microcontroller
b) Microcontroller and microcomputer
c) Hardwired and microprocessor control
d) Hardwired and microprogrammed control

(1 mark)

Q11 Below are the steps of a possible operation of a processor, EXCEPT:
a) Fetch, Decode, Execute
b) Fetch, Decode, Execute, Write Back
c) Fetch, Decode, Execute, Erase
d) Fetch, Decode, Execute, Store

(1 mark)

Q12 A program counter _____.
a) generates the control signals to execute an instruction.
b) enables the efficient handling of a micro program subroutine.
c) point out the next instruction to be executed.
d) sequentially averages all instructions in the control memory.

(1mark)

Q13 The performance of a pipelined processor suffers if _____.
a) consecutive instructions are dependent on each other
b) the pipeline stages share hardware resources
c) the pipelined stages have different delays
d) all the above

(1 mark)

Q14 For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
a) ISA
b) Multiple cycle design
c) Super-scalar design
d) All the mentioned

(1 mark)

Q15 If a processor clock is rated as 1250 million cycles per second, then its clock period is _____.

a) $8 * 10^{-10}$ sec
b) $1.6 * 10^{9}$ sec
c) $1.9 * 10^{-10}$ sec
d) $1.25 * 10^{-10}$ sec

(1 mark)

Q16 Any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline. As a result, some operation must be delayed, and the pipeline stalls. This condition called _____.

a) Instruction hazard
b) Peripheral hazard
c) Structural hazard
d) Memory hazard

(1 mark)

Q17 Processors can achieve an instruction execution throughput of more than one instruction per cycle called _____.

a) ultrascalar processor
b) multiscalar processor
c) superscalar processor
d) microscalar processor

(1 mark)

Q18 The execution time T of a program that has a dynamic instruction count N is given by:

$$T = \frac{N \times S}{R}$$

where S is the average number of clock cycles it takes to fetch and execute one instruction, and R is the _____.

a) clock rate
b) signal rate
c) number of stages
d) number of instructions

(1 mark)

Q19 Data hazard can be solved in software using:

a) data forwarding
b) stall the pipeline at a particular clock cycle
c) compiler to insert independent or No Operation instructions
d) separate time for read and write operation involving the data

(1 mark)

Q20 Branch prediction methods can be one of the following except:

a) static
b) fixed
c) dynamic
d) schedule

(1 mark)

Q21 Methods to reduce branch penalty are as follows except:
a) stall the pipeline
b) branch prediction
c) delayed slot branch
d) instruction prefetching

(1 mark)

Q22 A memory management technique used to improve computer performance is .
a) storing as much data as possible on disk
b) selecting memory chips based on their cost
c) using the cache to store data that will most likely be needed soon
d) preventing data from being moved from the cache to primary memory

(1 mark)

Q23 How many 32kB RAM chips are needed to provide a memory capacity of 256kB?
a) 8
b) 32
c) 64
d) 128

(1 mark)

Q24 A computer's memory is composed of 4K words of 32 bits each. How many total bits in memory?
a) 12800
b) 131072
c) 1280000
d) 1310720

(1 mark)

Q25 The maximum addressing capacity of a microprocessor which uses 16-bit database and 32-bit address base is _____.
a) 32 MB
b) 64 MB
c) 4 GB
d) 8 GB

(1mark)

Q26 A computer's memory is composed of 8K words of 32 bits each, and a byte is 8 bits. How many bytes does this memory contain?
a) 4K
b) 8K
c) 16K
d) 32K

(1 mark)

Q27 The effectiveness of the cache memory is based on the property of _____
a) Memory size
b) Clock rate
c) Locality of reference
d) None of the mentioned

(1 mark)

Q28 A memory organisation that can hold up to 1024 bits and has a minimum of 10 address lines can be organised into _____.

a) 128 X 8
b) 256 X 4
c) 512 X 2
d) 1024 X 1

(1 mark)

Q29 The main aim of virtual memory organisation is

i. To provide effective memory access
ii. To provide better memory transfer
iii. To improve the execution of the program

a) i and ii
b) i and iii
c) ii and iii
d) i, ii and iii

(1 mark)

Q30 The disadvantage of the EEPROM is/are _____

a) The Latency in read operation
b) The inefficient memory mapping schemes used
c) The requirement of different voltages to read, write and store information
d) All the above

(1 mark)

Q31 The standard SRAM chips are costly as _____

a) They house six transistors per chip
b) They require specially designed PCB's
c) They use highly advanced micro-electronic devices
d) None of the mentioned

(1 mark)

Q32 A CPU generally handles interrupt by executing an interrupt service routine _____.

a) as soon as an interrupt is raised
b) by checking the interrupt register at fixed time intervals
c) by checking the interrupt register at the end of fetch cycle
d) by checking the interrupt register after finishing the execution of the current instruction

(1 mark)

Q33 An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as _____.

a) DDA
b) DMA
c) serial interface
d) BR (Bus Request)

(1 mark)

Q34 Suppose a processor does not have any stack pointer register. Which of the following statements is true?

a) It cannot have subroutine call instruction.
b) Nested subroutine calls are possible, but interrupts are not.
c) All sequences of subroutine calls and interrupts are possible.
d) It can have subroutine call instruction, but no nested subroutine calls.

(1 mark)

Q35 Interrupts form an important part in _____ systems.

a) real-time processing
b) memory
c) CPU
d) bus

(1 mark)

Q36 Interrupts can be generated in response to _____.

i. detected program errors such as arithmetic overflow or division by zero
ii. detected hardware faults
iii. input/output activities
iv. internal timers

a) i, ii, and iv
b) i, iii, and iv
c) ii, iii, and iv
d) i, ii, iii, and iv

(1 mark)

Q37 When the process is returned after an interrupt service _____ should be loaded again.

i. Condition codes
ii. Register contents
iii. Return addresses
iv. Stack contents

a) i and ii
b) i and iv
c) iii and iv
d) ii, iii, and iv

(1 mark)

Q38 The most important objective of the USB is to provide _____

i. Asynchronous data transfer
ii. Easy device connection
iii. Isochronous transmission
iv. Plug and play

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv

(1 mark)

Q39 Three (3) types of bus lines including _____.

a) Address, Control, and Data lines
b) Address, Data, and I/O lines
c) Address, Control, and I/O lines
d) Control, Data, and I/O lines

(1 mark)

Q40 The maximum bus speed is largely limited by follows, distinguish the incorrect answer.

a) The type of the bus.
b) The length of the bus.
c) The number of devices on the bus.
d) The need to support a range of devices.

(1 mark)

SECTION B: 6 Subjective Questions (60 marks)

Q41 **Figure Q41** shows the Instruction Cycle State Diagram. The execution cycle for a particular instruction may involve more than one reference to memory. Also, instead of memory references, an instruction may specify an I/O operation. The figure is in the form of a state diagram. For any given instruction cycle, some states may be null and others may be visited more than once.

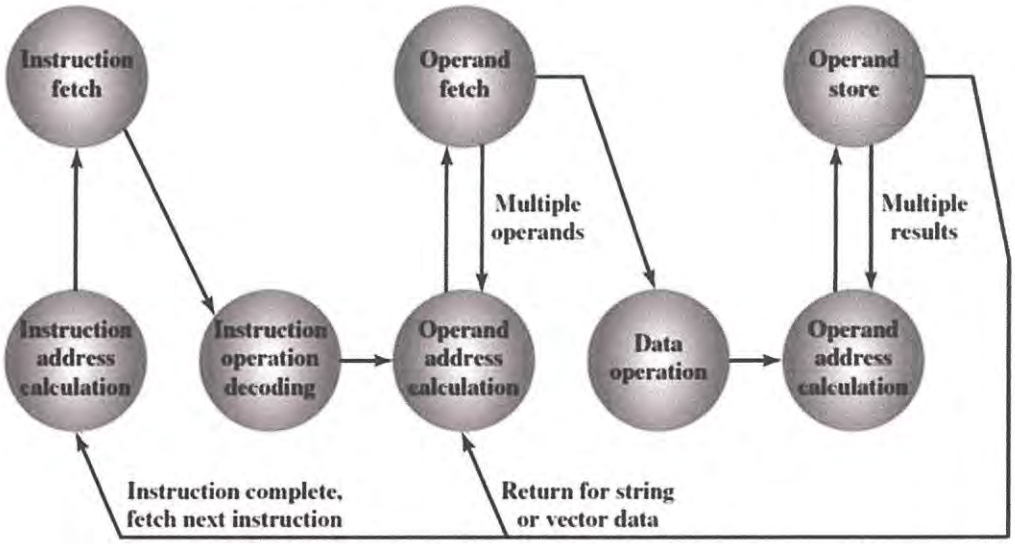

Figure Q41

(a) Based on **Figure Q41**, describe the task done in the following states:

(i) Instruction fetch

(ii) Instruction operation decoding

(iii) Operand fetch

(iv) Data operation

(4 marks)

(b) The operation of the processor's hardware components is governed by control signals. These signals determine which multiplexer input is selected, what operation is performed by the ALU, etc. There are two basic approaches on how the processor generates the control signals that cause the fetch and execute actions to take place in the correct sequence and at the right time.

(i) State the two basic approaches on how the processor generates the control signal.

(2 marks)

(ii) Explain the advantage and the disadvantage for each of the approach.

(4 marks)

Q42 Assume that a machine with clock rate 200MHz is running a program that use Arithmetic Logic: ADD, MUL, DIV and STORE instruction. All the instructions need to be executed in order to complete that program. The following measurements are recorded on that machine.

Instruction	**Total Instruction**	**Number of Cycle Needed to Execute One Instruction**
STORE	4×10^6	3
DIV	2×10^6	4
MUL	8×10^6	2
ADD	10×10^6	1

Calculate:

(a) Total instruction being executed in that program.

(3 marks)

(b) Total cycle to complete the execution of that program.

(3 marks)

(c) Total Cycle per Instruction (CPI) of that program.

(3 marks)

(d) The Million Instruction per Cycle (MIPS) of that program.

(3 marks)

(e) Total execution time.

(3 marks)

Q43 (a) Differentiate between DRAM and SRAM in terms of its application.

(2 marks)

(b) Compare the characteristic of DRAM and SDRAM in term of speed, size and cost.

(3 marks)

(c) Elaborate the similarity between EPROM and Flash memory in term of its data erasing technology.

(3 marks)

(d) Consider a dynamic RAM that must be given a refresh 64 000 times per second. Each refresh operation requires 150 ns. Calculate the time required to refresh the memory in one minute.

(2marks)

Q44 Consider a memory with features in **Table Q44 (a)** and **Table Q44 (b).**

Table Q44 (a)

Memory Type	Clock Cycle
Level 1 cache	2
Level 2 cache	6
Level 3 cache	8
DDR SDRAM	143
Hard disk	178

Table Q44 (b)

Item	Value
Total Number of L2 Cache accessed by CPU	50 access
Total Number of Hit	45 access
Hit Time	7 ns

(a) By using the features as in **Table Q44 (a),** determine the miss penalty in nanoseconds when a Level 3 cache miss occurs, and the data is found in DDR SDRAM. Assume that the duration for 1 clock cycle is 3 ns.

(2 marks)

(b) By using the features as in **Table Q44(a)** and **Table Q44(b),** calculate the Average Memory Access Time of the system

(3 marks)

Q45 (a) Correlate how the shared bus architectures give advantage when connecting many devices.

(2 marks)

(b) Analyse the performance impact of synchronous and asynchronous bus timing when many devices are connected to the bus.

(4 marks)

(c) Differentiate between program-controlled I/O and interrupt-driven I/O in terms of CPU computational efficiency.

(2 marks)

(d) For an I/O device that requires high throughput data transfer to and from a CPU, determine the suitable bus protocol between PCI and USB. Justify your answer.

(2 marks)

Q46 Digital currency and online payments system become popular since this transaction operating independently of a central bank.

i. With the aid of suitable diagram (Infographic), illustrate how the Blockchain works.

(6 marks)

ii. List 4 applications can be used Blockchain technology.

(4 marks)

– END OF QUESTIONS –